



Compal Confidential

QBL60 Schematics Document

AMD Sabine

APU Llano / Hudson M2_M3 / Vancouver Whistler

UMA only / PX Muxless with BACO

2010-02-21

LA-7552P REV: 0.1

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Model Name : QBL60



Sabine

VRAM 1G/2G
128M16 x 4/8
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DDR3

Thermal Sensor
ADM1032
page 19

ATI Vancouver Whistler

uFCBGA-962

Page 18~22

GFX x 8 Gen2

GFX x 4

APU HDMI
(UMA / Muxless)

DP x1 (DP0 TXP/N0)

AMD FS1 APU

Llano

uPGA-722 Package

Page 6~10

Memory BUS(DDR3)

Dual Channel

1.5V DDRIII 800~1333MHz

204pin DDRIII-SO-DIMM X2

BANK 0, 1, 2, 3

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HDMI Conn.
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LVDS Conn.
Reserve eDP
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LVDS

Travis LVDS
Translator
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CRT Conn.
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FCH CRT (VGA DAC)

FCH

Hudson-M2/M3

uFCBGA-656

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GPP1

GPP0

MINI Card 1
WLAN
page 32

LAN(GbE)
BCM57785
page 29

RJ45
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Umi

USB2
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USB2
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USB2
(LS-7322P)
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CMOS
Camera
page 27

Mini Card
(with BT)
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Card Reader
RTS5137
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USB
3.3V 48MHz

Port 0

Port 1

Port 5

Port 2

Port 3

Port 4

HD Audio 3.3V 24.576MHz/48Mhz

S-ATA Gen2

port 0

port 1

SATA HDD1
Conn.
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ODD
Conn.
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HDA Codec
ALC269
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ENE KB930

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Touch Pad
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Int.KBD
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LED
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RTC CKT.
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DC/DC
Interface CKT.
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Power Circuit
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External board

LS-7326P
Power/B
page 35

LS-7322P
Audio BD
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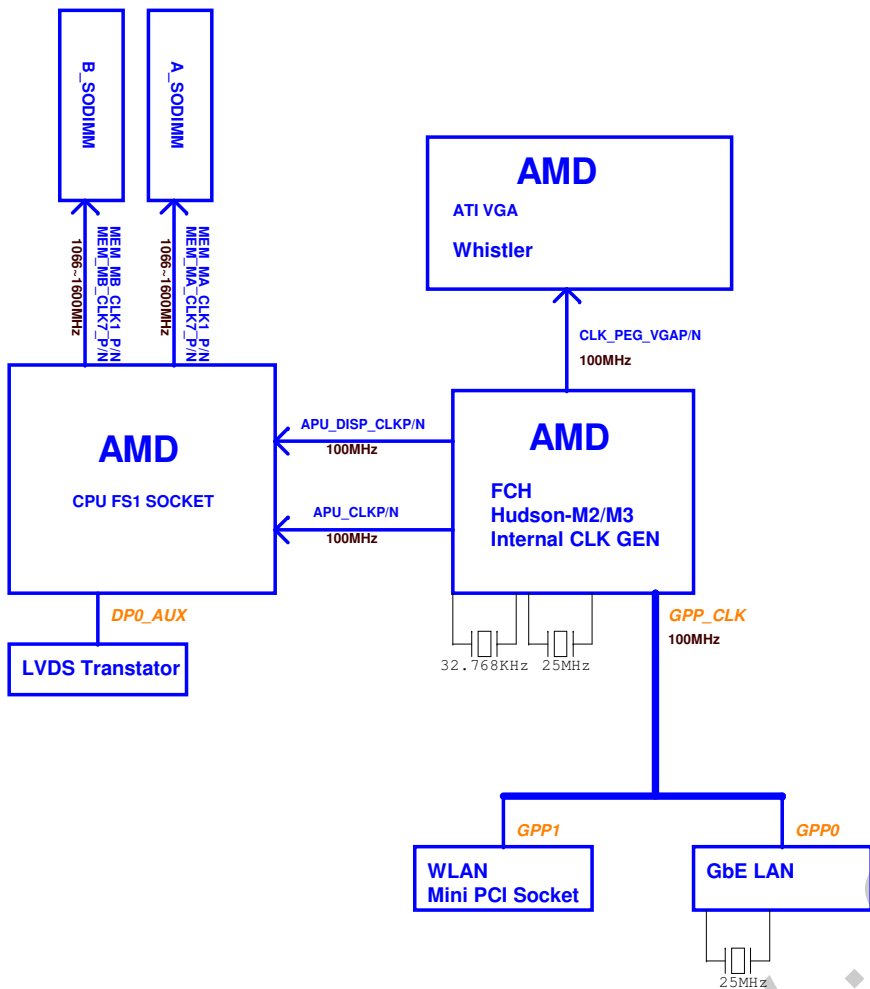
BIOS ROM

SYS BIOS (2M)
page 15

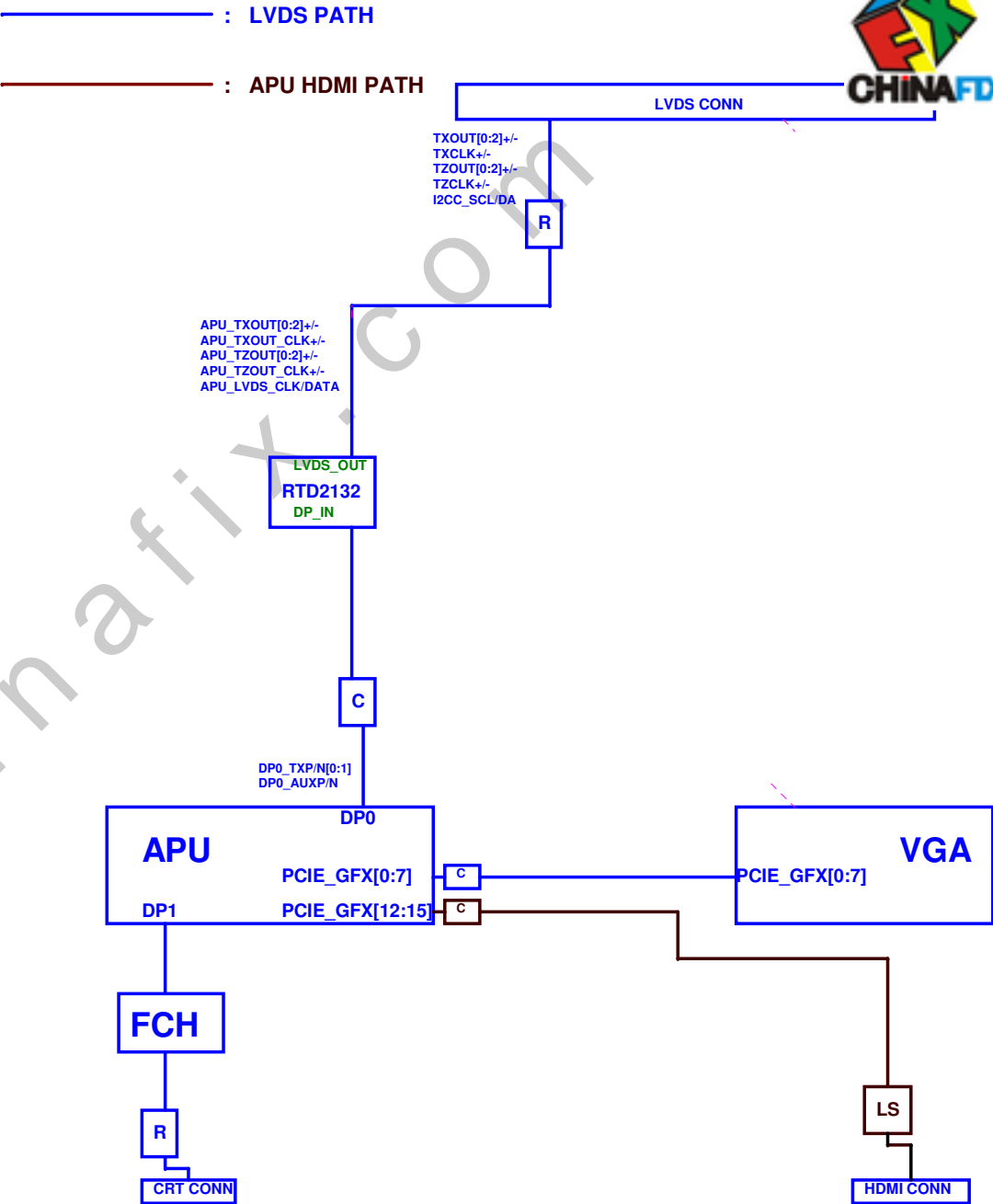
EC BIOS (128K)
page 35

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CLOCK DISTRIBUTION



DISPLAY DISTRIBUTION



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Voltage Rails

Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.

x = 1 is read cmd, x= 0 is writee cmd.

External PCI Devices

Device	IDSEL#	REQ#/GNT#	Interrupts

EC SM Bus1 address

EC SM Bus2 address

Device	Address	HEX	Device	Address	HEX
Smart Battery	0001 011X b	16H	ADI ADM1032 (VGA)	1001 101X b	9AH
			(APU)		
			RTD2132S (TL)		

FCH
SM Bus 0 address

FCH
SM Bus 1 address

Device	Address	HEX	Device	Address	HEX
DDR DIMM1	1101 000X b	D0			
DDR DIMM2	1101 001X b	D2			

STATE \ SIGNAL	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1 (Power On Suspend)	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	LOW	ON	OFF	OFF	OFF

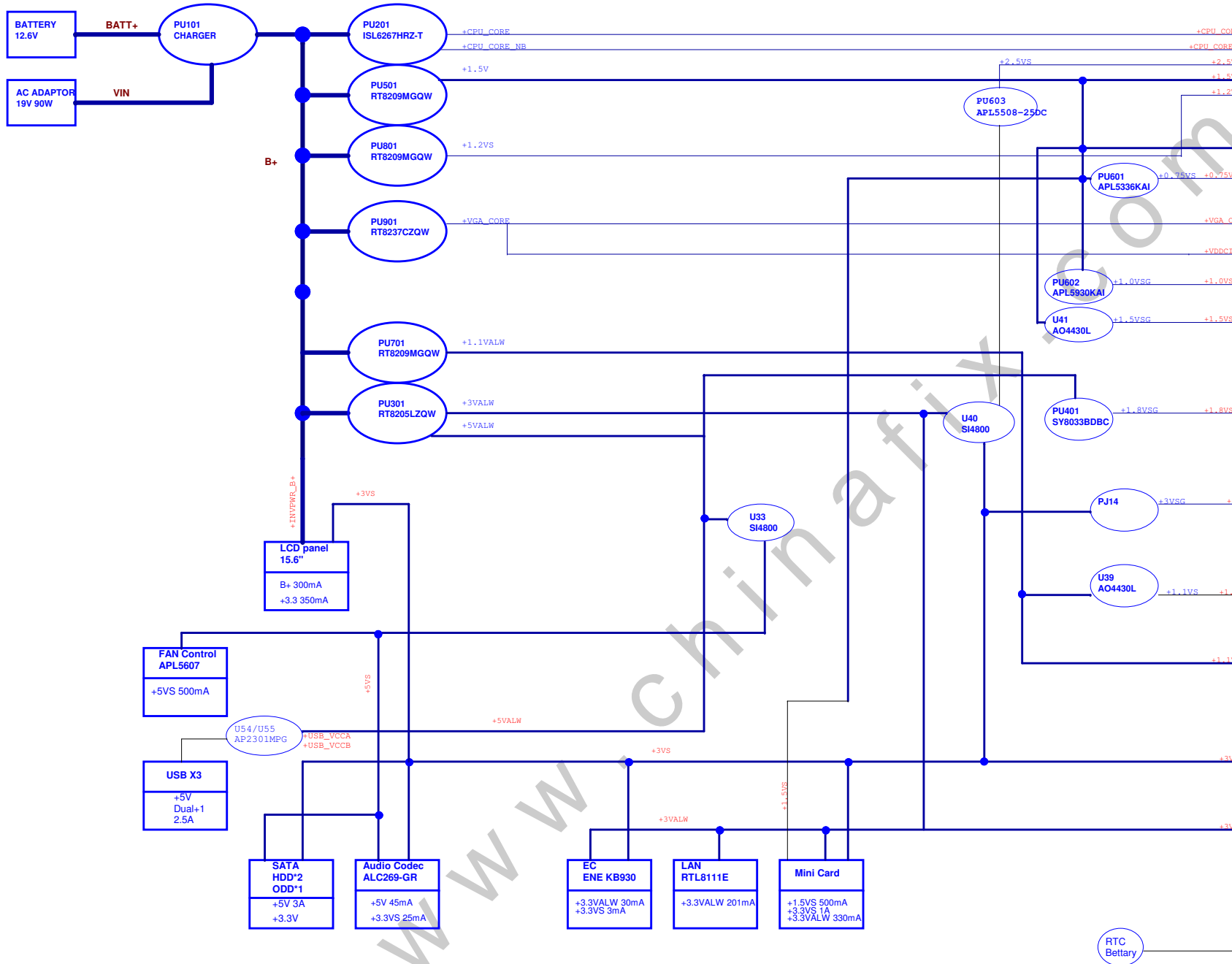
BTO Option Table

[illegible]

BOM Config

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AMD APU FS1	
0.7~1.475V	VDD CORE 54A
0.7~1.475V	VDDNB 27.5A
+2.5VS	VDDA 500mA
+1.5V	VDDIO 4.6A
+1.2VS	VDDR 6.7A

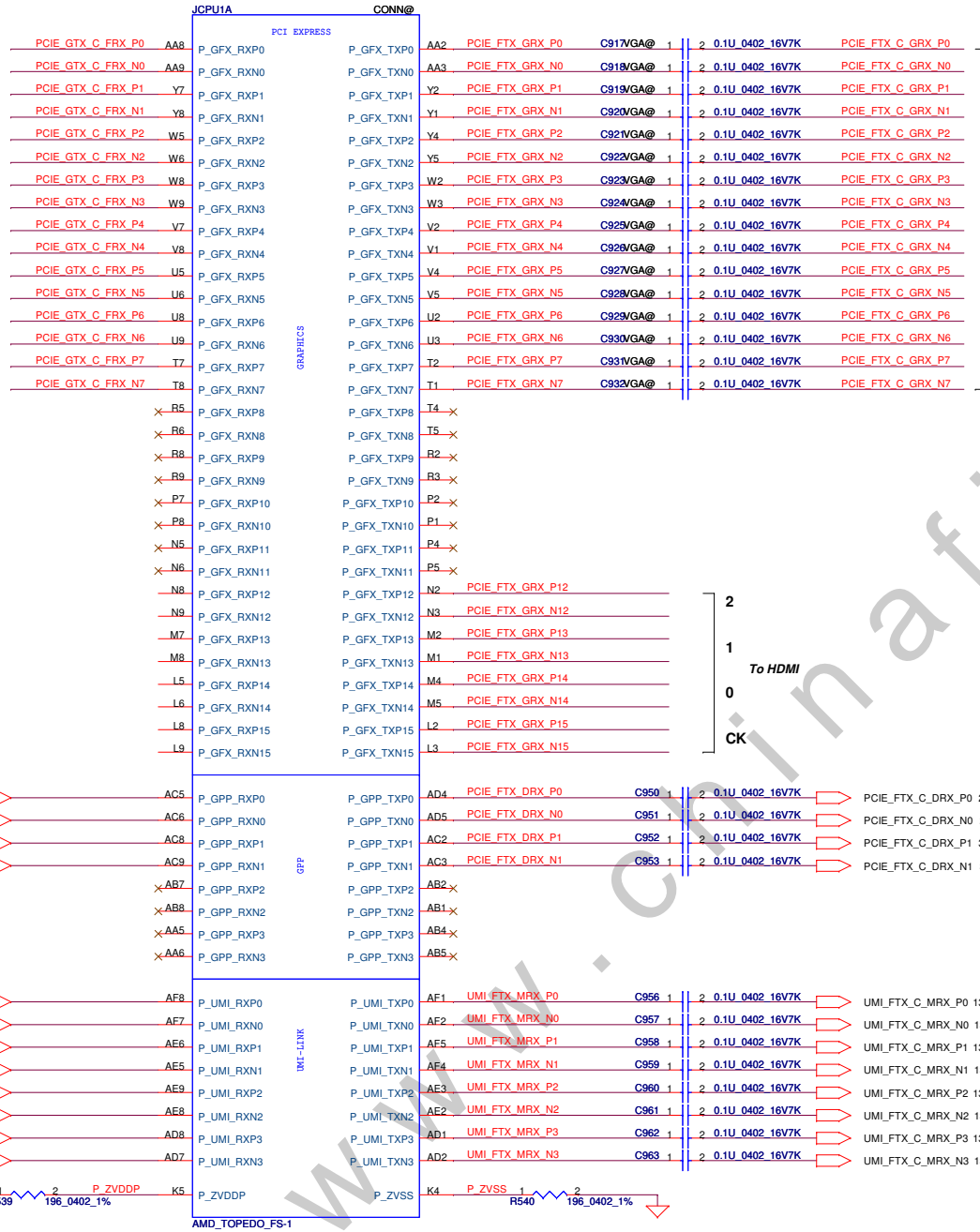
RAM DDRIII SODIMMX2	
+1.5V	VDD_MEM 4A
+0.75VS	VTT_MEM 0.5A

VGA ATI Whistler/Seymour/Granville	
0.85~1.1V	VDDC 47A
0.9~1.0V	VDDCI 4.6A
+1.0VSG	DPLL_VDDC: 125 mA SPV10: 120 mA PCIE_VDDC: 2000 mA DP[A/E]_VDD10: 680 mA
+1.5VSG	VDDR1: 3400 mA
+1.8VSG	PLL_PVDD: 75 mA TSVDD: 20 mA AVDD: 70 mA VDD1D1: 100 mA VDD2D1: 50 mA A2VDDC: 1.5 mA VDD_CT: 110 mA VDDR4: 170 mA PCIE_PVDD: 40 mA MPV18: 150 mA SPV18: 75 mA PCIE_VDDR: 400 mA DP[A/F]_VDD18: 920 mA DP[A/F]_PVDD: 120 mA
+3VSG	A2VDD: 130 mA VDDR3: 60 mA

VRAM 1GB/2GB 64M / 128Mx16 * 4 / 8	
+1.5VSG	2.4 A

FCH AMD Hudson M2/M3	
+1.1VS	VDDPL_11_DAC: 7 mA VDDAN_11_ML: 226 mA VDDCR_11: 1007 mA VDDAN_11_CLK: 340 mA VDDAN_11_PCIE: 1088 mA VDDAN_11_SATA: 1337 mA
+1.1VALW	VDDAN_11_USB_S: 140 mA VDDCR_11_USB_S: 197 mA VDDAN_11_SSUSB_S: 282 mA VDDCR_11_SSUSB_S: 424 mA VDDCR_11_S: 187 mA VDDPL_11_SYS: 70 mA
+3VS	VDDIO_33_PCIEP: 131 mA VDDPL_33_SYS: 47 mA VDDPL_33_DAC: 20 mA VDDPL_33_ML: 20 mA VDDAN_33_DAC: 200 mA VDDPL_33_PCIE: 43 mA VDDPL_33_SATA: 93 mA VDDIO_AZ_S: 26 mA
+3VALW	VDDPL_33_SSUSB_S: 20 mA VDDPL_33_USB_S: 17 mA VDDAN_33_USB_S: 658 mA VDDIO_33_S: 59 mA VDDXL_33_S: 5 mA VDDAN_33_HWM_S: 12 mA
GND	VDDIO_33_GBE_S VDDCR_11_GBE_S VDDIO_GBE_S
RTC BAT	VDDBT_RTC_G

18 PCIE_GTX_C_FRX_P[0..7] 18
18 PCIE_GTX_C_FRX_N[0..7] 18



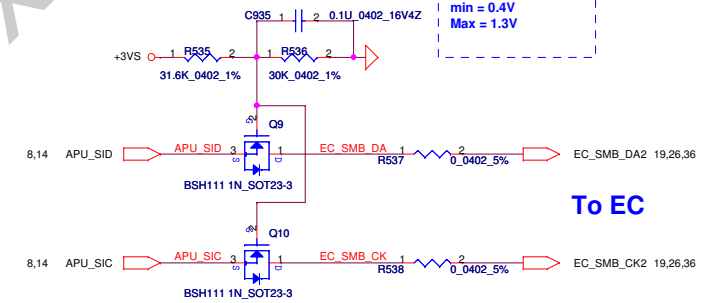
APU To HDMI

PCIE_FTX_GRX_P[12..15] 28
PCIE_FTX_GRX_N[12..15] 28

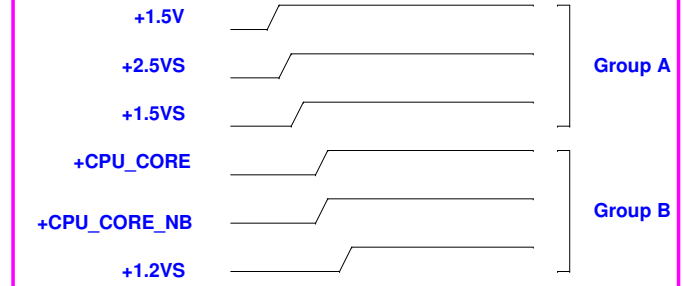


For UMA Mux.

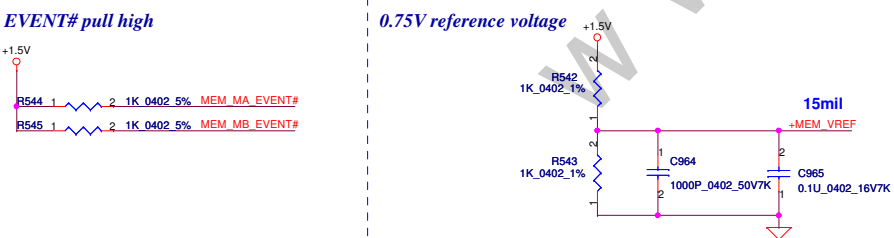
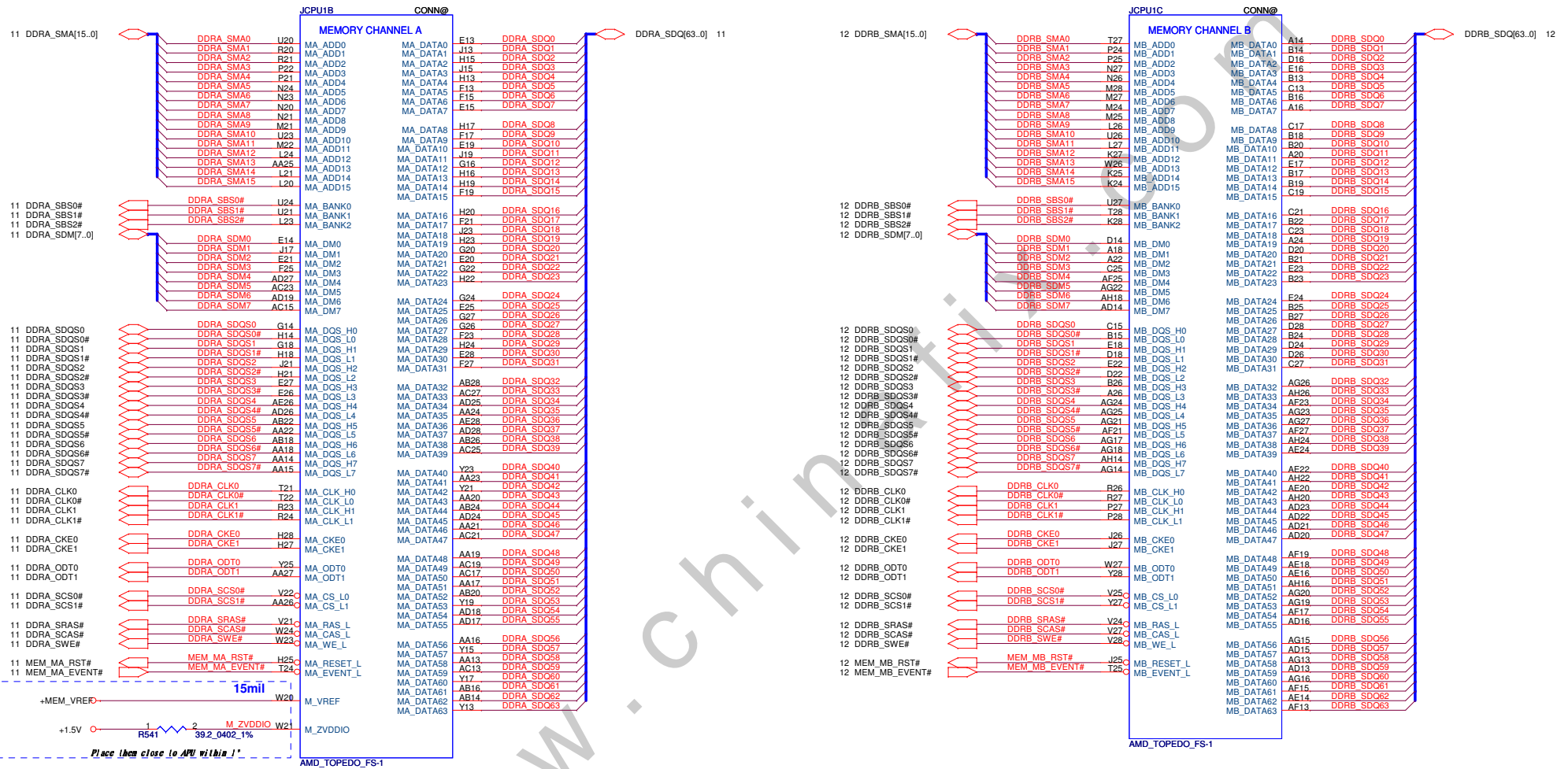
CPU TSI interface level shift



Power Sequence of APU



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To LVDS
Translator

To FCH VGA ML

100MHz

100MHz_NSS

TSI

Serial VID

Close to Header

Route as differential
with VSS_SENSE

APU_VDDNB_RUN_FB_L
APU_VDDNB_SEN route as differential

APU_VDD_RUN_FB_L
APU_VDD_SEN route as differential

Place near APU

Place near APU

System DP

TSI

Serial VID

Close to Header

Route as differential
with VSS_SENSE

APU_VDDNB_RUN_FB_L
APU_VDDNB_SEN route as differential

APU_VDD_RUN_FB_L
APU_VDD_SEN route as differential

JCPU1D

JCPU1D

System DP

TSI

Serial VID

Close to Header

Route as differential
with VSS_SENSE

APU_VDDNB_RUN_FB_L
APU_VDDNB_SEN route as differential

APU_VDD_RUN_FB_L
APU_VDD_SEN route as differential

AMD_TOPEDO_FS-1

CONN@

CONN@

System DP

TSI

Serial VID

Close to Header

Route as differential
with VSS_SENSE

APU_VDDNB_RUN_FB_L
APU_VDDNB_SEN route as differential

APU_VDD_RUN_FB_L
APU_VDD_SEN route as differential

AMD_TOPEDO_FS-1

Place near APU

Place near APU

System DP

TSI

Serial VID

Close to Header

Route as differential
with VSS_SENSE

APU_VDDNB_RUN_FB_L
APU_VDDNB_SEN route as differential

APU_VDD_RUN_FB_L
APU_VDD_SEN route as differential

AMD_TOPEDO_FS-1

Place near APU

Place near APU

System DP

TSI

Serial VID

Close to Header

Route as differential
with VSS_SENSE

APU_VDDNB_RUN_FB_L
APU_VDDNB_SEN route as differential

APU_VDD_RUN_FB_L
APU_VDD_SEN route as differential

AMD_TOPEDO_FS-1

To LVDS
Translator

To FCH

AUX 2-5 are for GFX interface
use, they could be selected to I2C
or AUX logic

VDDIO level
Need Level shift

VDDIO level
Need Level shift

VDDIO level
Need Level shift

VDDIO level
Need Level shift

VDDIO level
Need Level shift

VDDIO level
Need Level shift

VDDIO level
Need Level shift

VDDIO level
Need Level shift

VDDIO level
Need Level shift

If not used, pins are left unconnected (DG ref.)
20101111

DP0_AUXP R554 2 1.8K 040
DP0_AUXN R555 2 1.8K 040
ML_VGA_AUXP R547 2 1.8K 040
ML_VGA_AUXN R556 2 1.8K 040

TEST25_L R548 2 510 0402 1%
TEST25_H R557 2 510 0402 1%
TEST35 R558 1 300 0402 5%
M_TEST R564 1 39.2 0402 1%
FS1R1 R571 2 10K 0402 5%

FS1R1: Control S5 Dual PWR plane
in laptop, seems no use

ALLOW_STOP R612 1 2 1K 0402 5%
APU_RST# R577 1 2 1K 0402 5%
APU_PWRGD R578 1 2 300 0402 5%
APU_PWRGD R580 1 2 300 0402 5%

MISC

Asserted as an input to force the
processor into the HTC-active state

APU_PROCHOT# R591 1 0.0402 5%
THERMTRIP shutdown
temperature: 125 degree
APU_THERMTRIP# R616 1 1K 0402 5%
H_THERMTRIP# R611 1 0.0402 5%

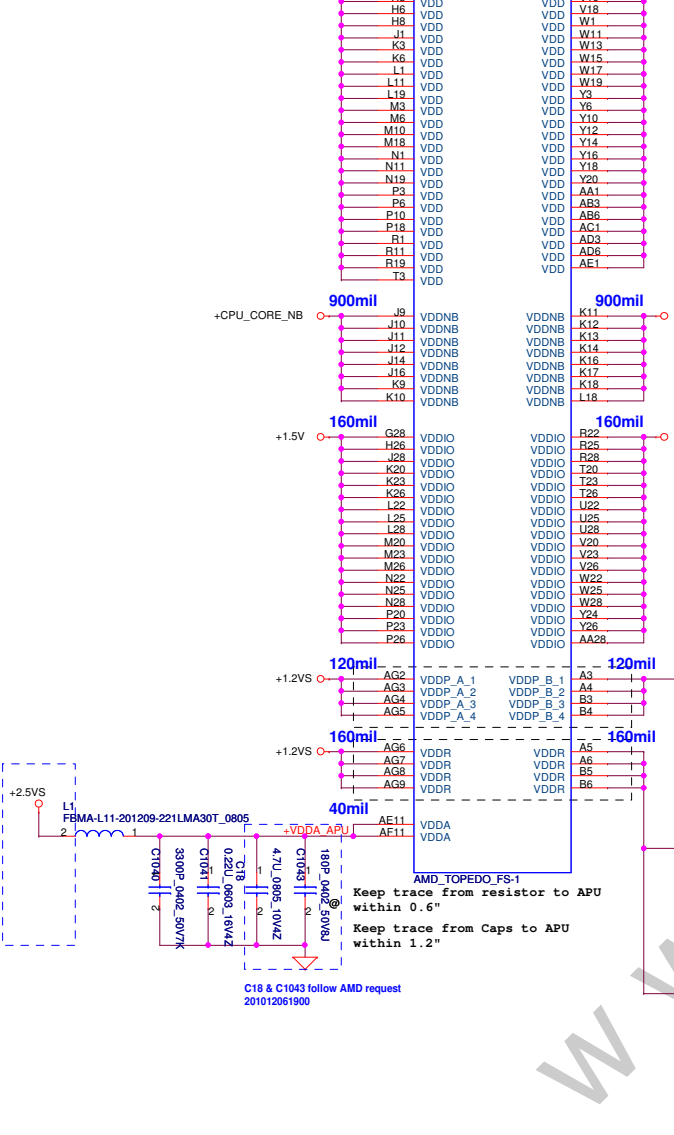
HDT Debug conn

APU_TCK R598 2 0.0402 5%
APU_TMS R599 2 0.0402 5%
APU_TDI R600 2 0.0402 5%
APU_TDO R601 2 0.0402 5%
APU_DBRDY R602 2 0.0402 5%
APU_RST# R603 2 0.0402 5%
APU_PWRGD R604 2 0.0402 5%
APU_TEST19 R605 2 0.0402 5%
APU_TEST18 R606 2 0.0402 5%

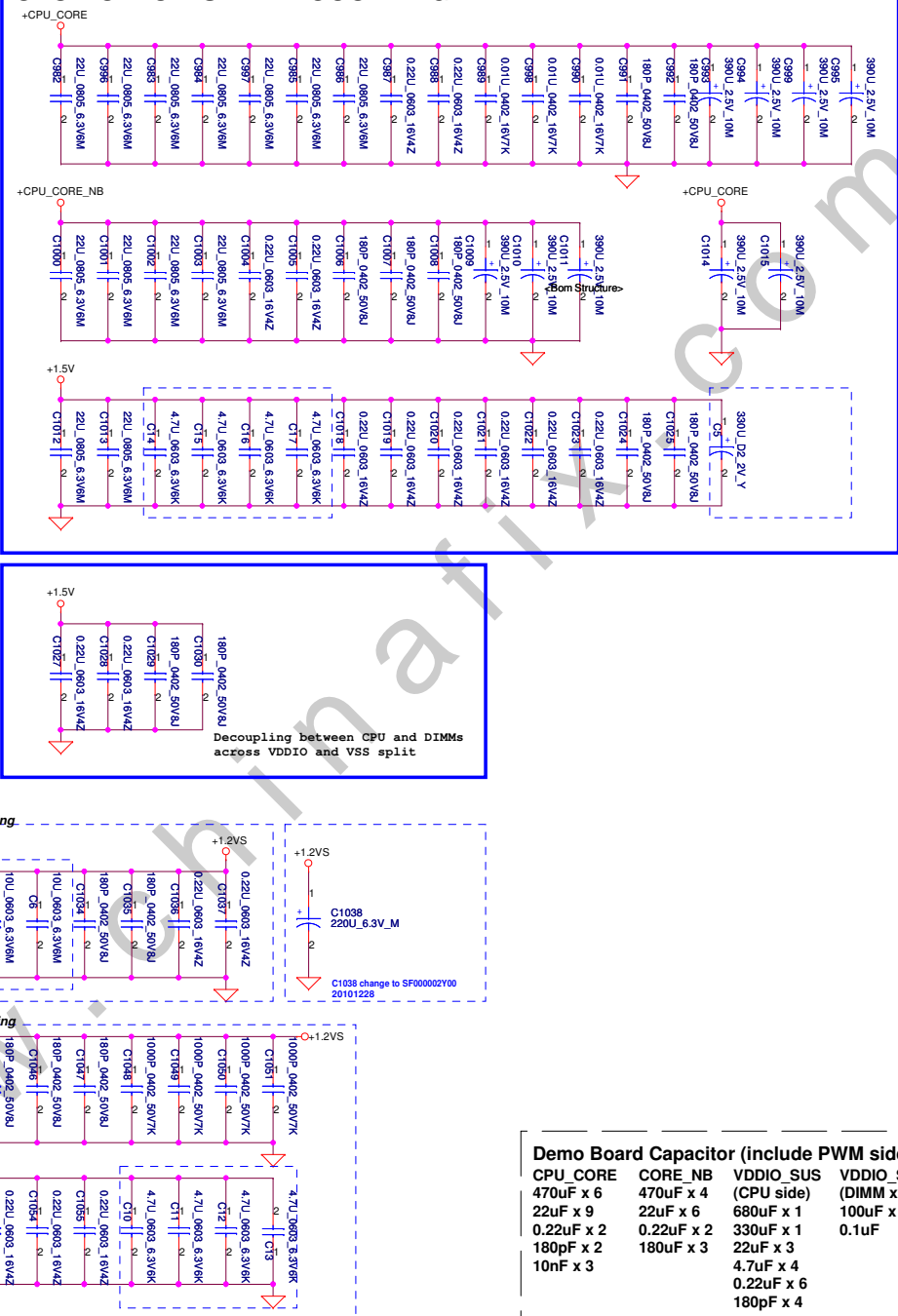
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Power Name	Consumption
VDD +CPU_CORE	50A
VDDNB +CPU_CORE_NB	22.5A
VDDIO +1.5V	4A
VDDP / VDDR +1.2VS	3A / 3.5A
VDDA +2.5VS	0.75A

CORE_NB 330uF X 2 22uF X 4	CPU_CORE 330uF X 4 22uF X 11
----------------------------------	------------------------------------



CPU BOTTOM SIDE DECOUPLING



JCPU1F	CONN@
A7	VSS
A15	VSS
A16	VSS
A17	VSS
A19	VSS
A21	VSS
A23	VSS
A25	VSS
B7	VSS
C4	VSS
C10	VSS
C14	VSS
C16	VSS
C18	VSS
C20	VSS
C22	VSS
C24	VSS
C26	VSS
C28	VSS
D13	VSS
D15	VSS
D17	VSS
D19	VSS
D21	VSS
D23	VSS
D25	VSS
D27	VSS
E4	VSS
E10	VSS
E12	VSS
F3	VSS
F11	VSS
F14	VSS
F16	VSS
F18	VSS
F20	VSS
F22	VSS
F24	VSS
F26	VSS
F28	VSS
G4	VSS
G8	VSS
G13	VSS
G15	VSS
G17	VSS
G19	VSS
G21	VSS
G23	VSS
G25	VSS
J4	VSS
J8	VSS
J12	VSS
J20	VSS
J22	VSS
J24	VSS
K18	VSS
L4	VSS
L7	VSS
L10	VSS
M9	VSS
M11	VSS
M19	VSS
N4	VSS
N7	VSS
N10	VSS
N18	VSS
P9	VSS
P11	VSS
P19	VSS
R4	VSS
R7	VSS
R10	VSS
R18	VSS
T9	VSS
T11	VSS
T14	VSS
U4	VSS
U7	VSS
U10	VSS
U18	VSS
V9	VSS
V11	VSS
V19	VSS
W4	VSS
W7	VSS
W10	VSS
W12	VSS
W14	VSS
W16	VSS
W18	VSS
Y9	VSS
Y22	VSS
AA4	VSS
AA7	VSS
AB9	VSS
AB13	VSS
AB15	VSS
AB17	VSS
AB19	VSS
AB21	VSS
AB23	VSS
AB25	VSS
AB27	VSS
AC4	VSS
AC7	VSS
AC10	VSS
AC12	VSS
AC14	VSS
AC16	VSS
AC18	VSS
AC20	VSS
AC22	VSS
AC24	VSS
AC26	VSS
AC28	VSS
AD9	VSS
AD11	VSS
AE4	VSS
AE7	VSS
AE13	VSS
AE15	VSS
AE17	VSS
AE19	VSS
AE21	VSS
AE23	VSS
AE25	VSS
AE27	VSS
AF3	VSS
AF6	VSS
AF9	VSS
AF12	VSS
AF14	VSS
AF16	VSS
AF18	VSS
AF20	VSS
AF22	VSS
AF24	VSS
AF26	VSS
AG10	VSS
AH5	VSS
AH8	VSS
AH13	VSS
AH15	VSS
AH17	VSS
AH19	VSS
AH21	VSS
AH23	VSS
AH25	VSS

AMD_TOPEDO_FS-1

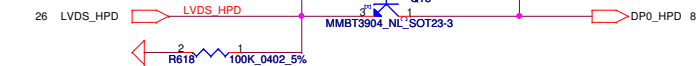
Demo Board Capacitor (include PWM side)						
CPU_CORE	CORE_NB	VDDIO_SUS	VDDIO_SUS	VDDP/R_PWM	VDDP	VDDR
470uF x 6	470uF x 4	(CPU side)	(DIMM x2)	470uF x 2	10uF x 3	4.7uF x 4
22uF x 9	22uF x 6	680uF x 1	100uF x 4	10uF x 1	0.22uF x 2	0.22uF x 4
0.22uF x 2	0.22uF x 2	330uF x 1	0.1uF		180pF x 2	1nF x 4
180pF x 2	180uF x 3	22uF x 3			4.7uF x 4	180pF x 4
10nF x 3		0.22uF x 6				
		180pF x 4				

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HPD

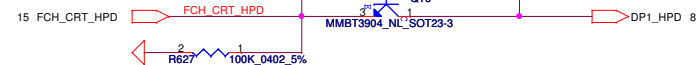
Translator HPD

From Translator



CRT HPD

From FCH

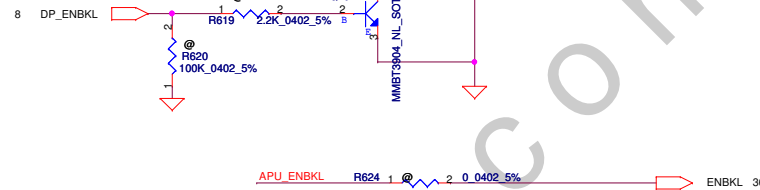


HDMI HPD

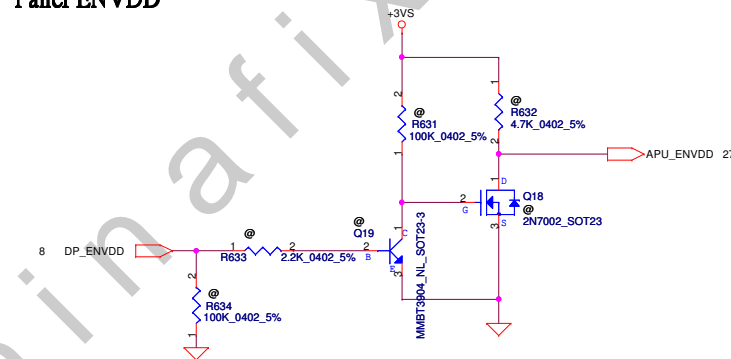
From HDMI Conn



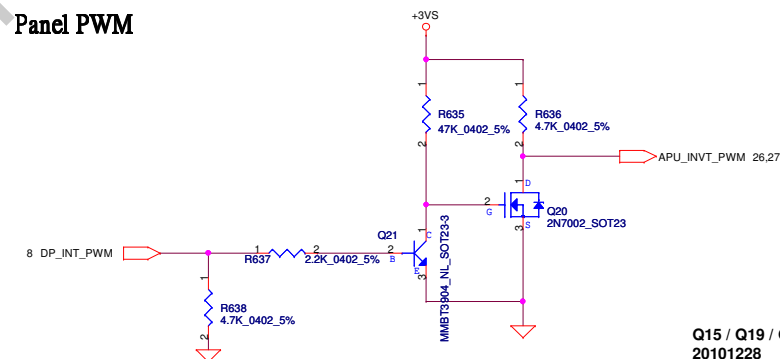
Panel ENBKL



Panel ENVDD



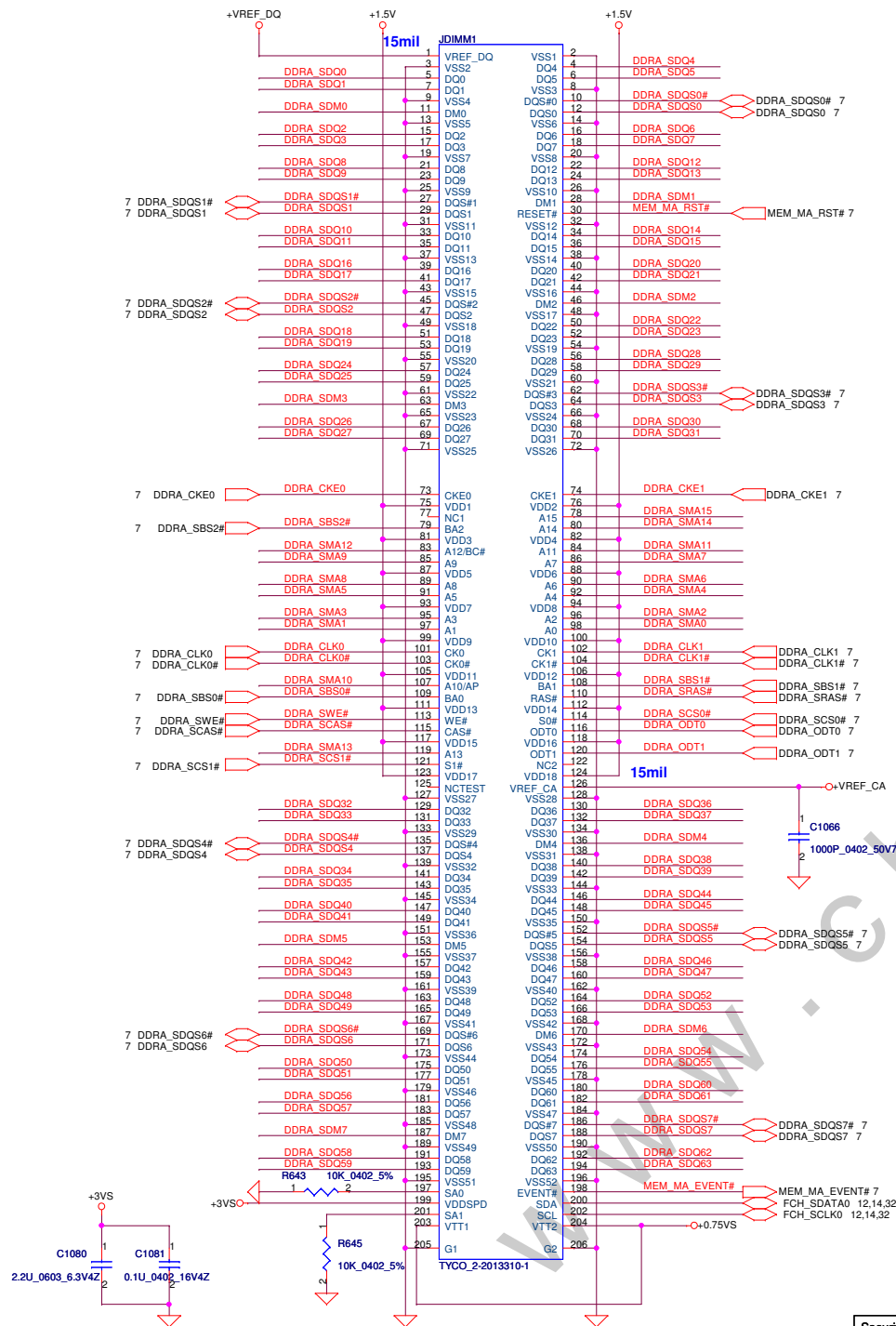
Panel PWM



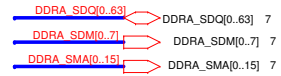
Q15 / Q19 / Q21 change to SB000006A00
20101228



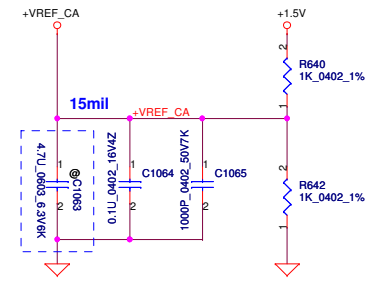
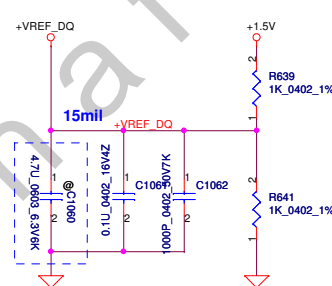
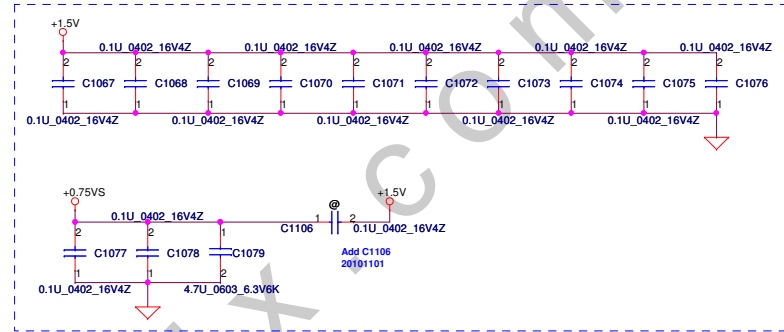
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				AMD FS1 Singal Level Shifter	
				Size	
				Document Number	
				QBL60 LA-7552P	
				Rev	
				0.1	
				Date	
				Wednesday, February 23, 2011	
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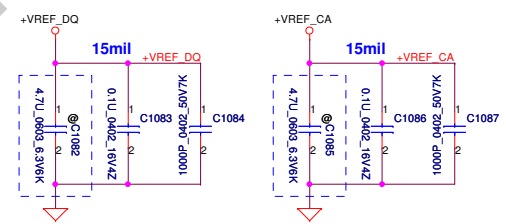
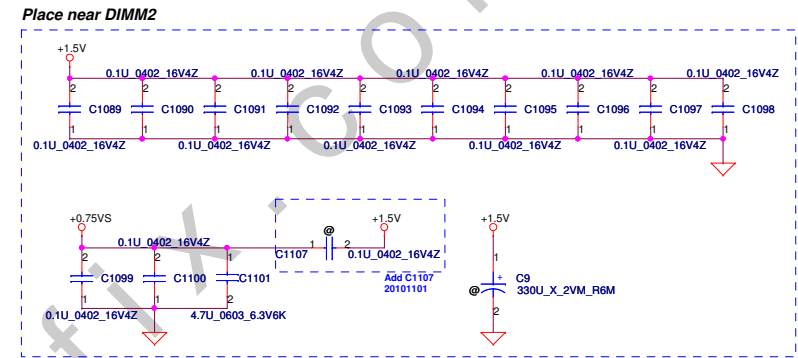
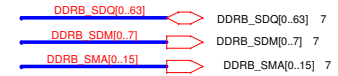
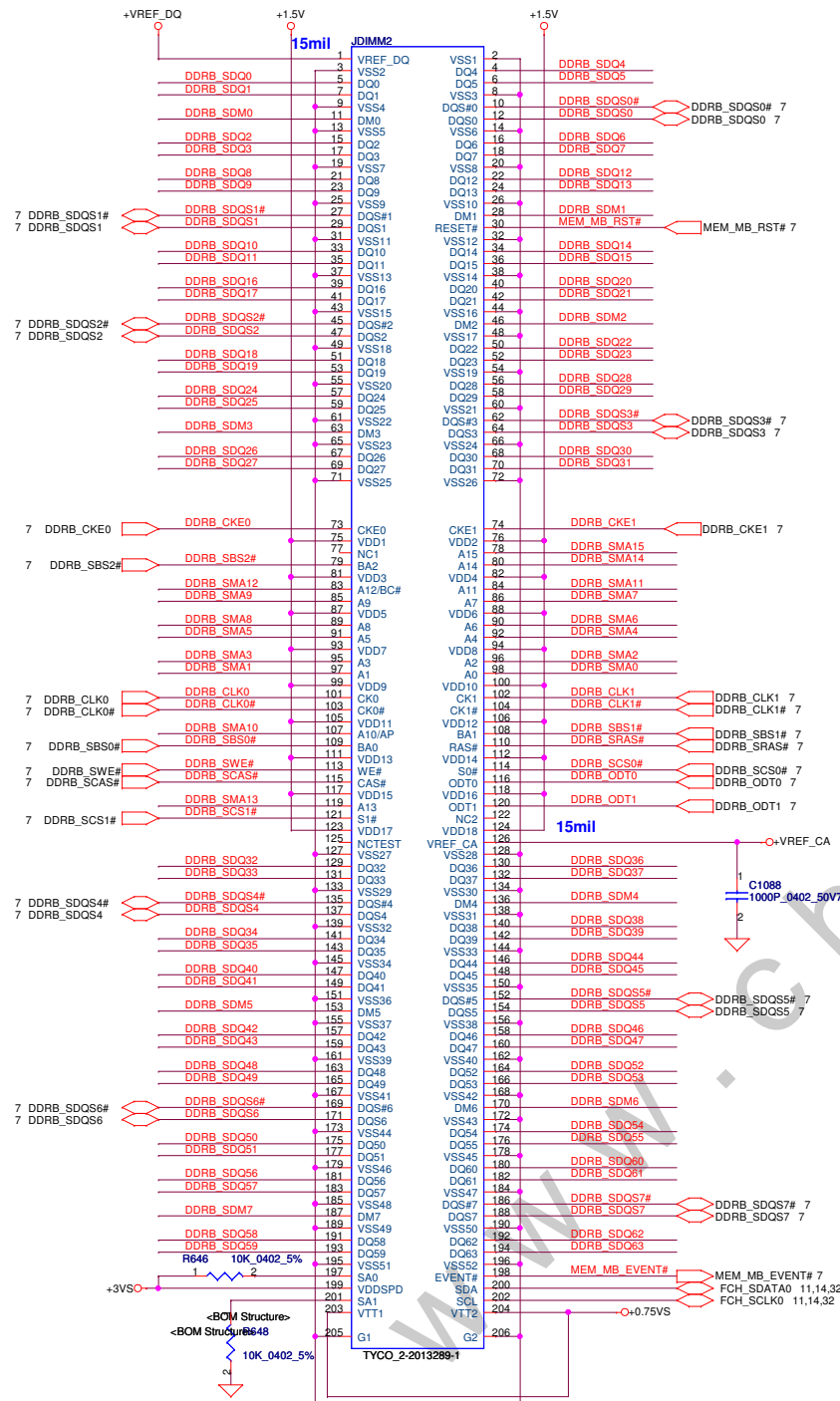
DIMM_A STD H:9.2mm
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Place near DIMM1

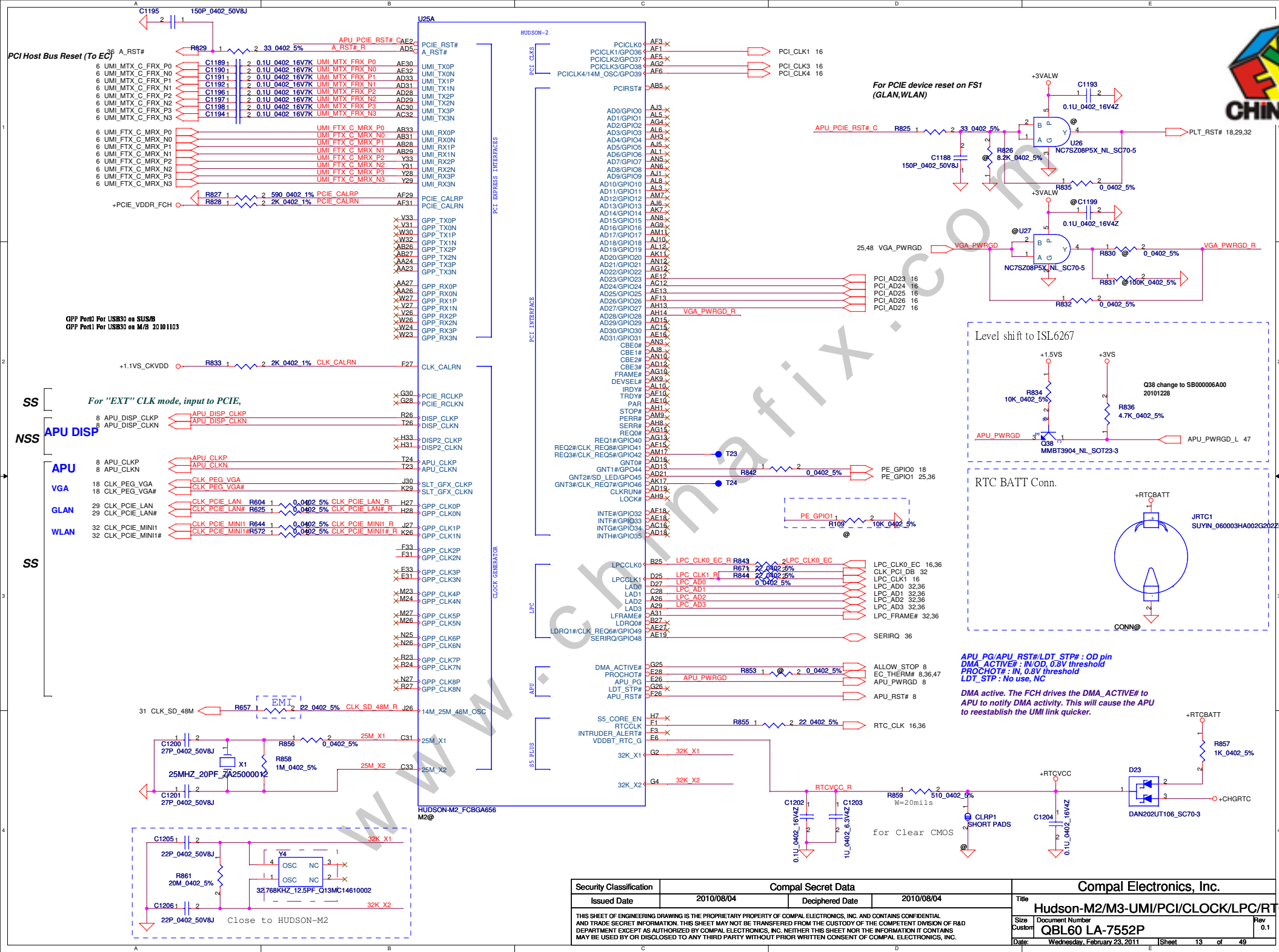


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DIMM_B STD H:5.2mm
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The schematic diagram illustrates the electrical architecture of the Hudson-M2/M3-UMI/PCI/CLOCK/LPC/RTC board. It details the connections for the CPU (Hudson-M2), PCI interface, LPC interface, and RTC. Key components and their connections include:

- CPU (Hudson-M2):** Shows various pins for PCI, LPC, and RTC interfaces, including clock signals and data lines.
- PCI Interface:** Details the connection to the PCI controller, including clock signals (PCI_CLK0, PCI_CLK1, PCI_CLK2, PCI_CLK3, PCI_CLK4) and data lines (PCI_D0, PCI_D1, PCI_D2, PCI_D3, PCI_D4, PCI_D5, PCI_D6, PCI_D7, PCI_D8, PCI_D9, PCI_D10, PCI_D11, PCI_D12, PCI_D13, PCI_D14, PCI_D15, PCI_D16, PCI_D17, PCI_D18, PCI_D19, PCI_D20, PCI_D21, PCI_D22, PCI_D23, PCI_D24, PCI_D25, PCI_D26, PCI_D27, PCI_D28, PCI_D29, PCI_D30, PCI_D31).
- LPC Interface:** Details the connection to the LPC controller, including clock signals (LPC_CLK0, LPC_CLK1, LPC_CLK2, LPC_CLK3, LPC_CLK4, LPC_CLK5, LPC_CLK6, LPC_CLK7, LPC_CLK8, LPC_CLK9, LPC_CLK10, LPC_CLK11, LPC_CLK12, LPC_CLK13, LPC_CLK14, LPC_CLK15, LPC_CLK16, LPC_CLK17, LPC_CLK18, LPC_CLK19, LPC_CLK20, LPC_CLK21, LPC_CLK22, LPC_CLK23, LPC_CLK24, LPC_CLK25, LPC_CLK26, LPC_CLK27, LPC_CLK28, LPC_CLK29, LPC_CLK30, LPC_CLK31).
- RTC:** Details the connection to the Real Time Clock, including the RTC_BATT connection and the RTC_CLK signal.
- Passive Components:** Includes resistors (R1, R2, R3, R4, R5, R6, R7, R8, R9, R10, R11, R12, R13, R14, R15, R16, R17, R18, R19, R20, R21, R22, R23, R24, R25, R26, R27, R28, R29, R30, R31, R32, R33, R34, R35, R36, R37, R38, R39, R40, R41, R42, R43, R44, R45, R46, R47, R48, R49, R50, R51, R52, R53, R54, R55, R56, R57, R58, R59, R60, R61, R62, R63, R64, R65, R66, R67, R68, R69, R70, R71, R72, R73, R74, R75, R76, R77, R78, R79, R80, R81, R82, R83, R84, R85, R86, R87, R88, R89, R90, R91, R92, R93, R94, R95, R96, R97, R98, R99, R100), capacitors (C1, C2, C3, C4, C5, C6, C7, C8, C9, C10, C11, C12, C13, C14, C15, C16, C17, C18, C19, C20, C21, C22, C23, C24, C25, C26, C27, C28, C29, C30, C31, C32, C33, C34, C35, C36, C37, C38, C39, C40, C41, C42, C43, C44, C45, C46, C47, C48, C49, C50, C51, C52, C53, C54, C55, C56, C57, C58, C59, C60, C61, C62, C63, C64, C65, C66, C67, C68, C69, C70, C71, C72, C73, C74, C75, C76, C77, C78, C79, C80, C81, C82, C83, C84, C85, C86, C87, C88, C89, C90, C91, C92, C93, C94, C95, C96, C97, C98, C99, C100), and inductors (L1, L2, L3, L4, L5, L6, L7, L8, L9, L10, L11, L12, L13, L14, L15, L16, L17, L18, L19, L20, L21, L22, L23, L24, L25, L26, L27, L28, L29, L30, L31, L32, L33, L34, L35, L36, L37, L38, L39, L40, L41, L42, L43, L44, L45, L46, L47, L48, L49, L50, L51, L52, L53, L54, L55, L56, L57, L58, L59, L60, L61, L62, L63, L64, L65, L66, L67, L68, L69, L70, L71, L72, L73, L74, L75, L76, L77, L78, L79, L80, L81, L82, L83, L84, L85, L86, L87, L88, L89, L90, L91, L92, L93, L94, L95, L96, L97, L98, L99, L100).

The diagram is organized into sections for different interfaces and components, with labels for pins, components, and values. A large watermark 'CHINA' is visible across the center of the diagram.

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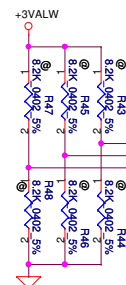
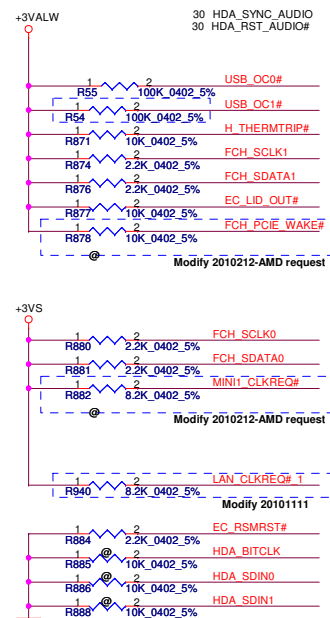
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Compal Electronics, Inc.
Hudson-M2/M3-UMI/PCI/CLOCK/LPC/RTC
QBL60 LA-7552P
Date: Wednesday, February 23, 2011 Sheet 13 of 49



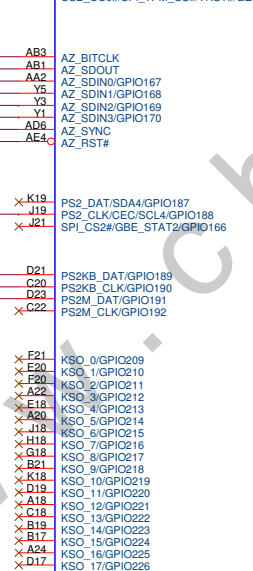
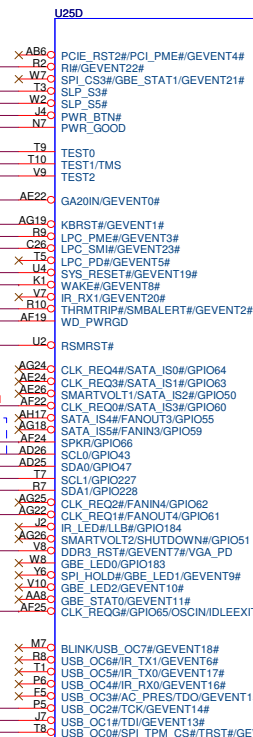
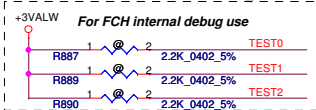
THERMTRIP:
Need level shift from +3VALW to +1.5V

SM bus 0-->S0 PWR domain
SM bus 1-->S5 PWR domain
VGA_PD: Support MLDAC power
save if connect
0: MLDAC power on
1: MLDAC power off



Project SKU ID	L(N)	H(YES)
GPIO189 (use VGA)	R46	R46
GPIO190 (use PX)	R46	R46
GPIO191	L(15")	H(17")

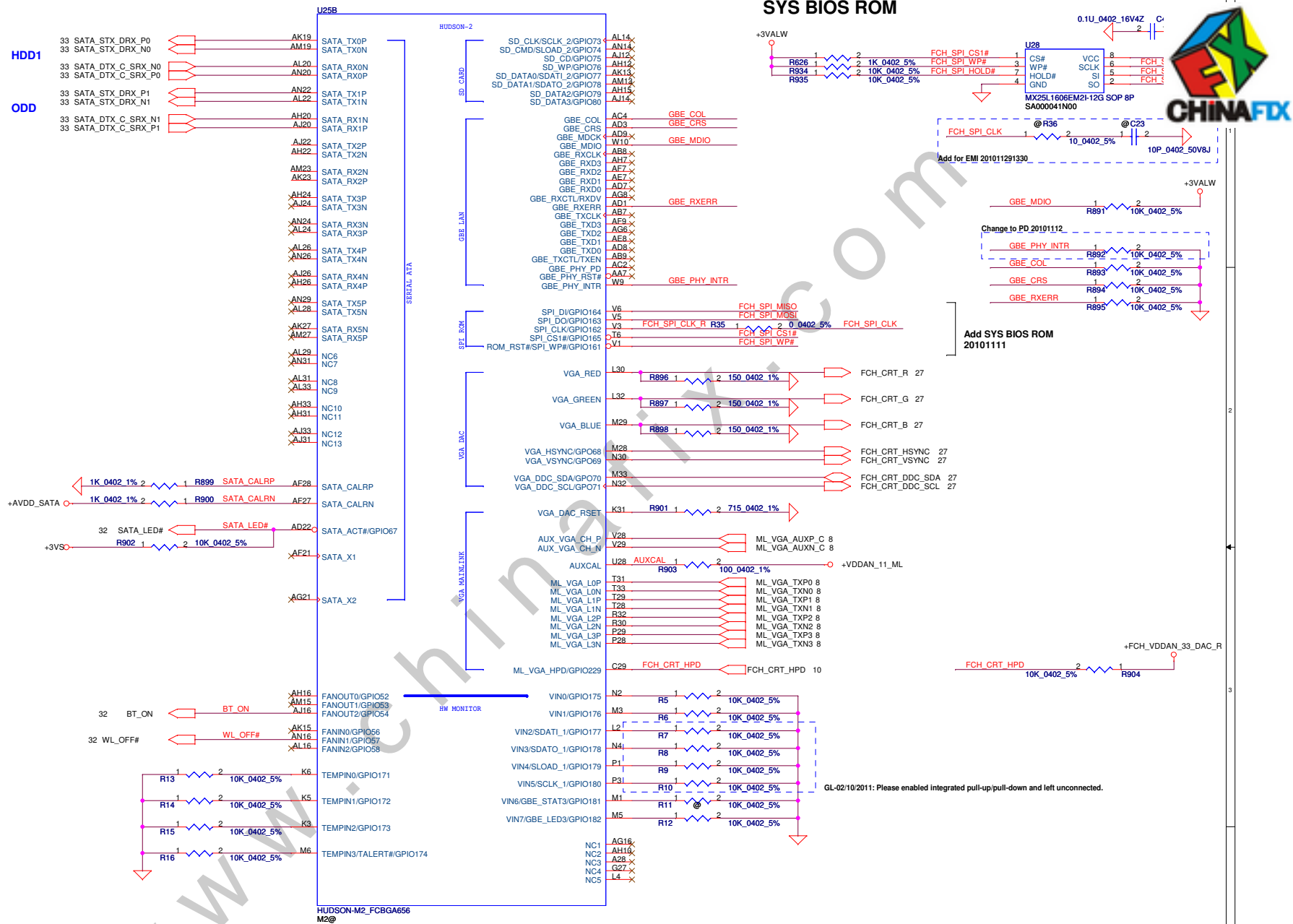
Add Project ID Table
201011301600



HUDSON-M2_FCBGA56

M2@

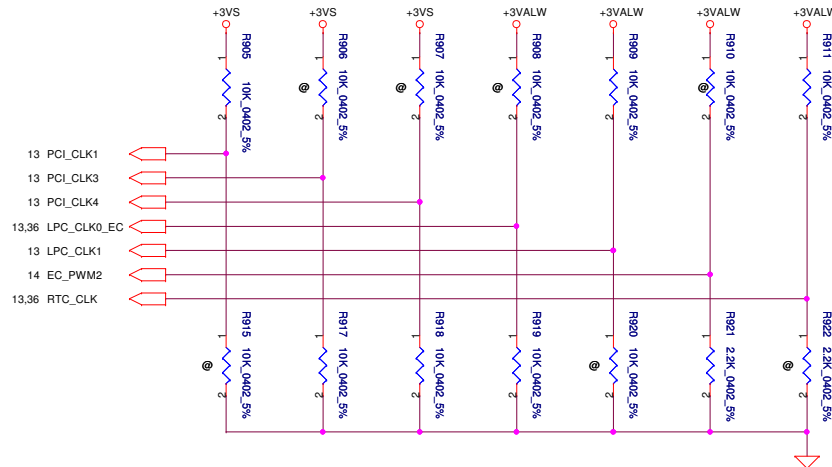
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				Custom	QBL60 LA-7552P
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STRAP PINS

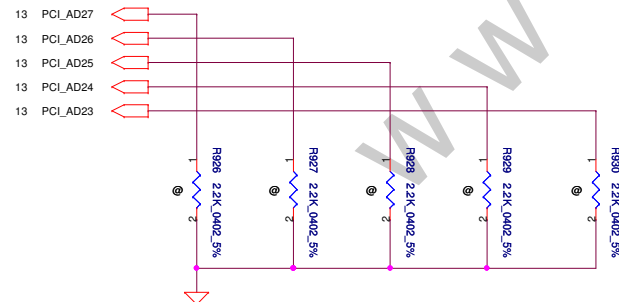
	PCI_CLK1	PCI_CLK3	PCI_CLK4	LPC_CLK0	LPC_CLK1	EC_PWM2	RTC_CLK
PULL HIGH	ALLOW PCIE GEN2 DEFAULT	USE DEBUG STRAPS	NON_FUSION CLOCK MODE	EC ENABLED	CLKGEN ENABLED DEFAULT	LPC ROM	S5 PLUS MODE DISABLED DEFAULT
PULL LOW	FORCE PCIE GEN1	IGNORE DEBUG STRAP DEFAULT	FUSION CLOCK MODE DEFAULT	EC DISABLED DEFAULT	CLKGEN DISABLE	SPI ROM DEFAULT	S5 PLUS MODE ENABLED



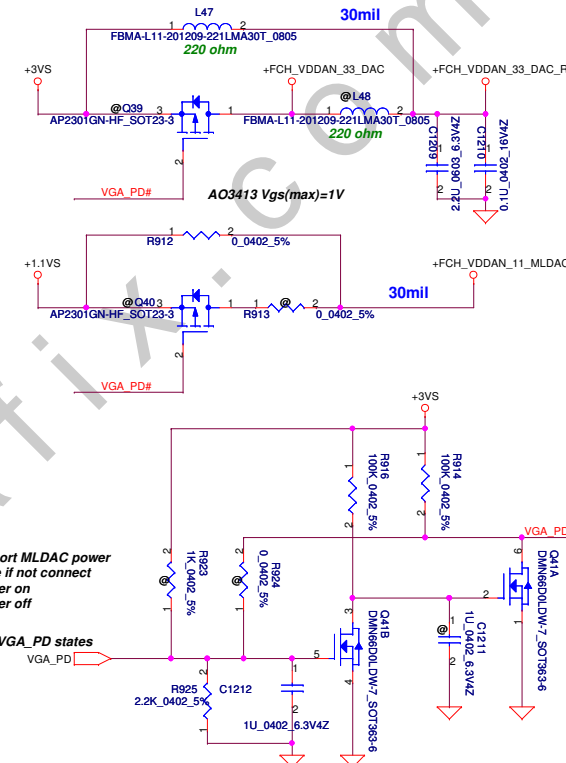
DEBUG STRAPS

FCH HAS 15K INTERNAL PU FOR PCI_AD[27:23]

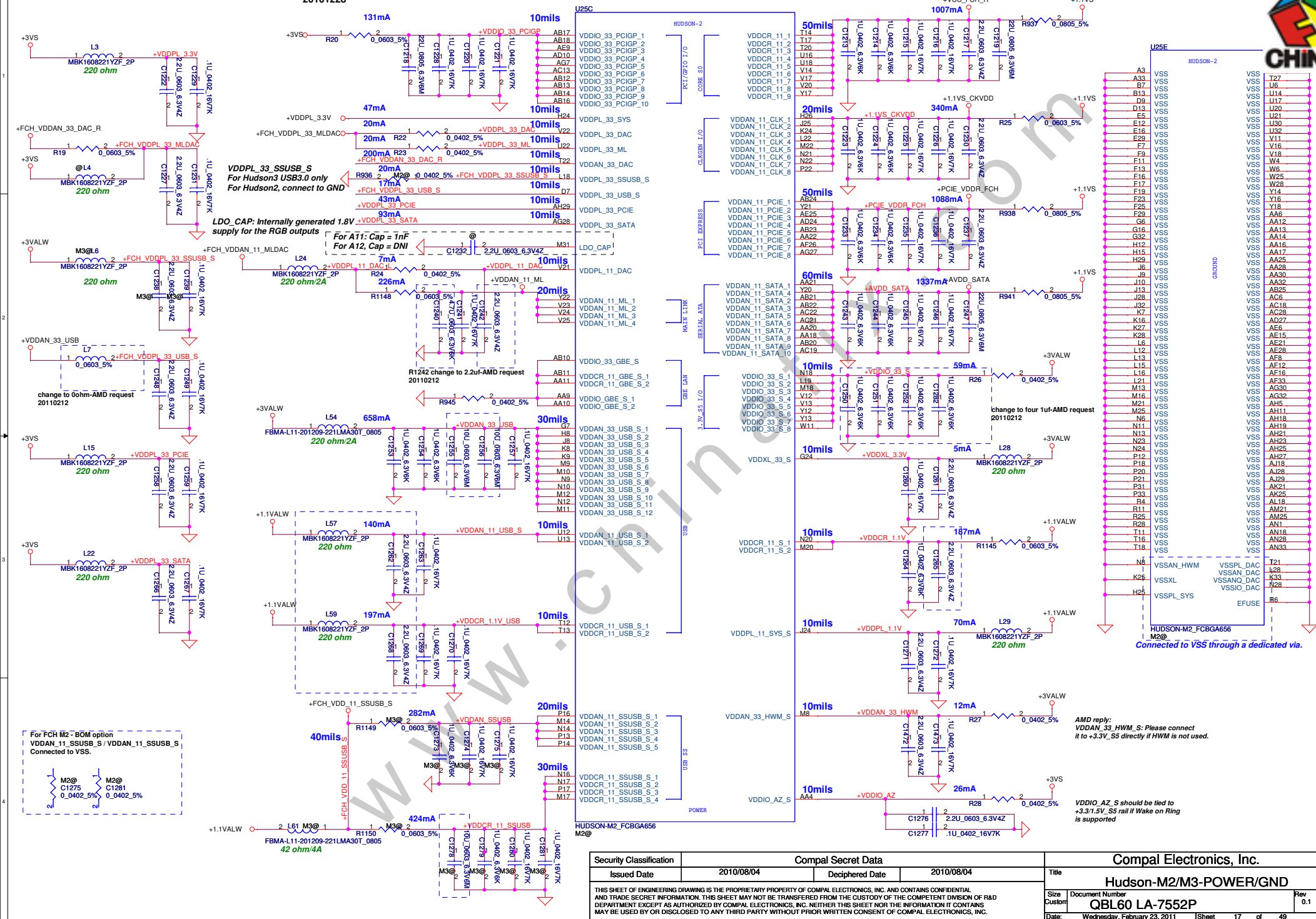
PCI_AD26	PCI_AD27		PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE PCI PLL DEFAULT	DISABLE ILA AUTORUN DEFAULT	USE FC PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	DISABLE PCI MEM BOOT DEFAULT
PULL LOW	BYPASS PCI PLL	ENABLE ILA AUTORUN	BYPASS FC PLL	USE EEPROM PCIE STRAPS	ENABLE PCI MEM BOOT



If support ML DAC power down when no VGA plug

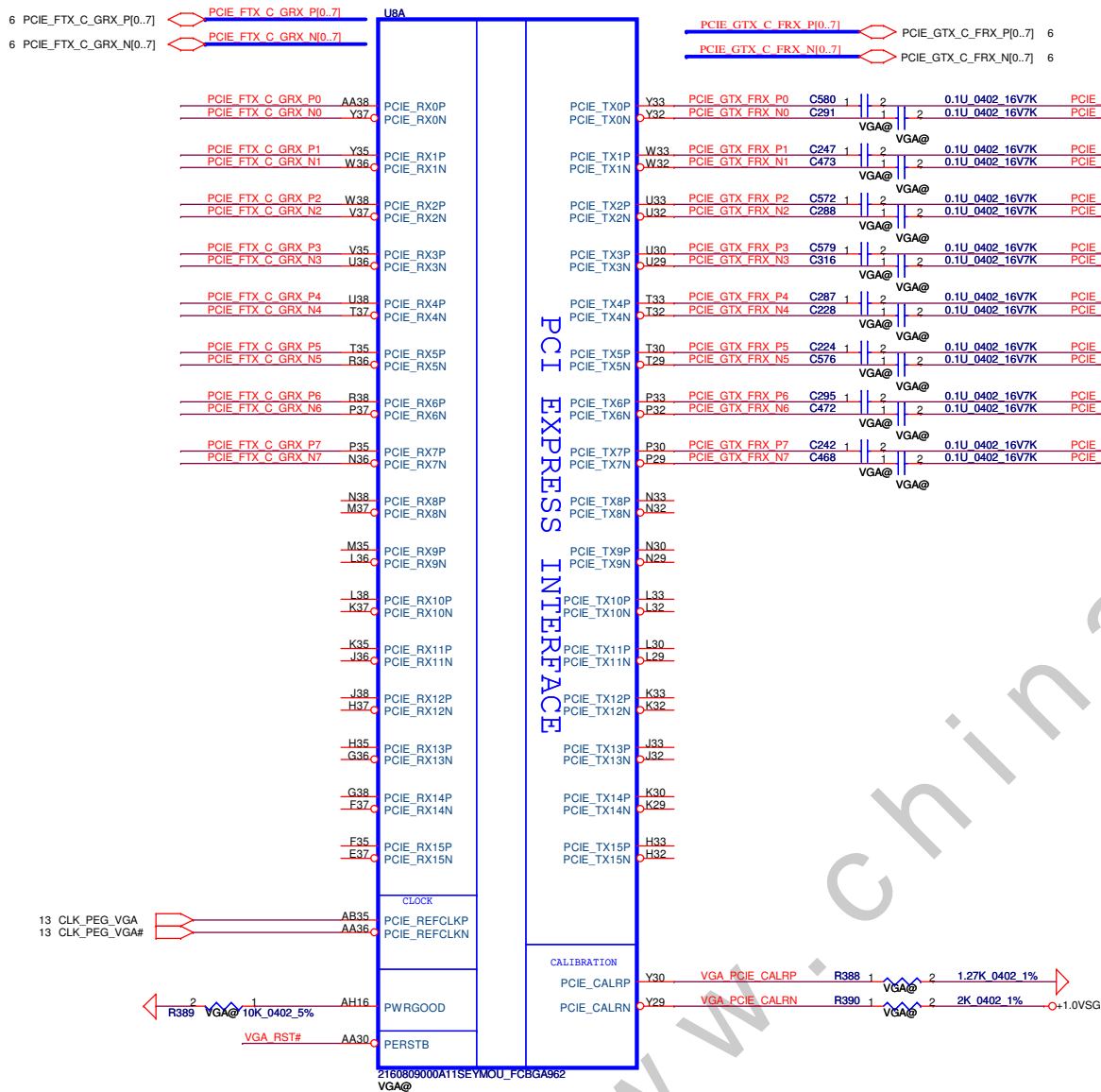


C1218 / C1219 / C1247 Change to SE00000110
20101228



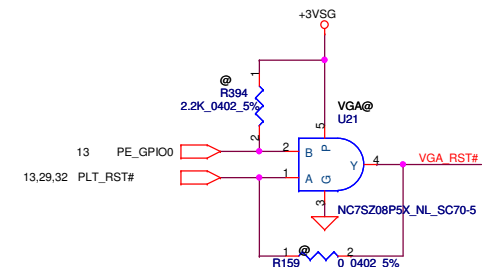
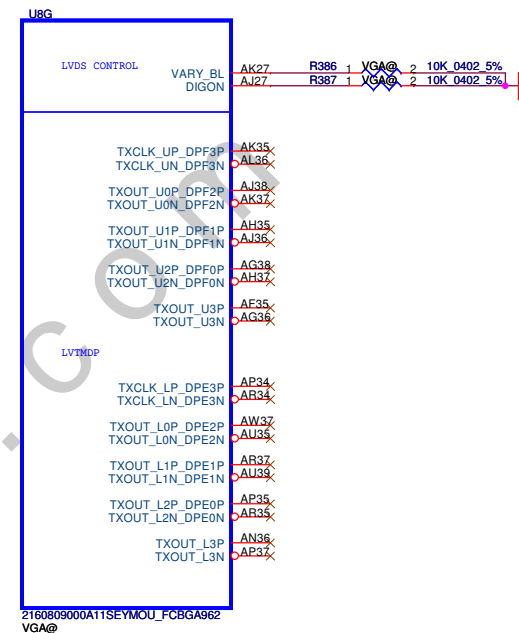
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GFX PCIE LANE REVERSAL



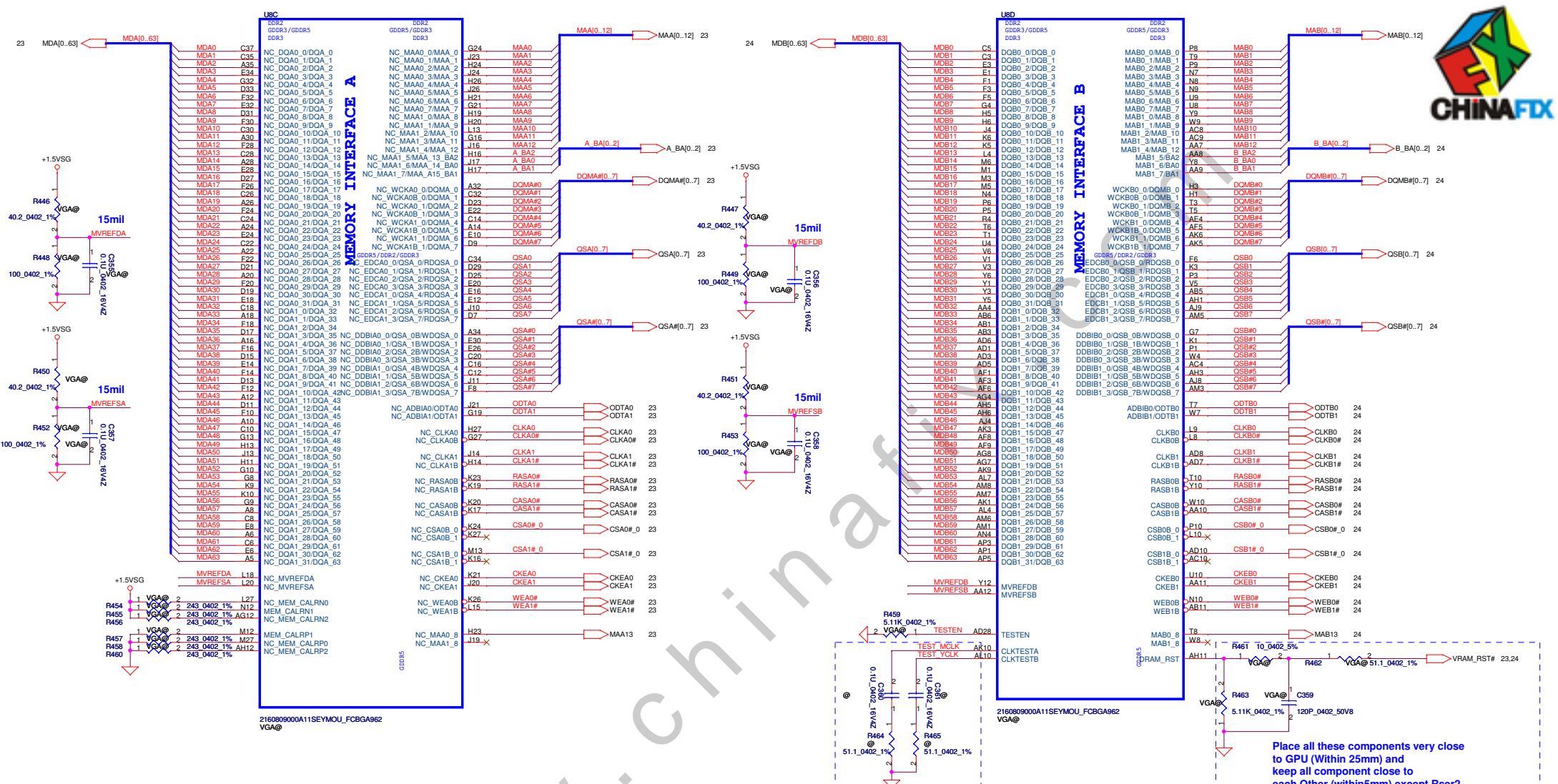
<DIGON>
Controls panel digital power on/off.
Active High ,external PD need

<VARY_BL>
LCD PWM (pulse width modulated)
output to adjust LCD brightness
Active High ,external PD need



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										Vancouver_PCIE / LVDS	
										Document Number	
										QBL60 LA-7552P	
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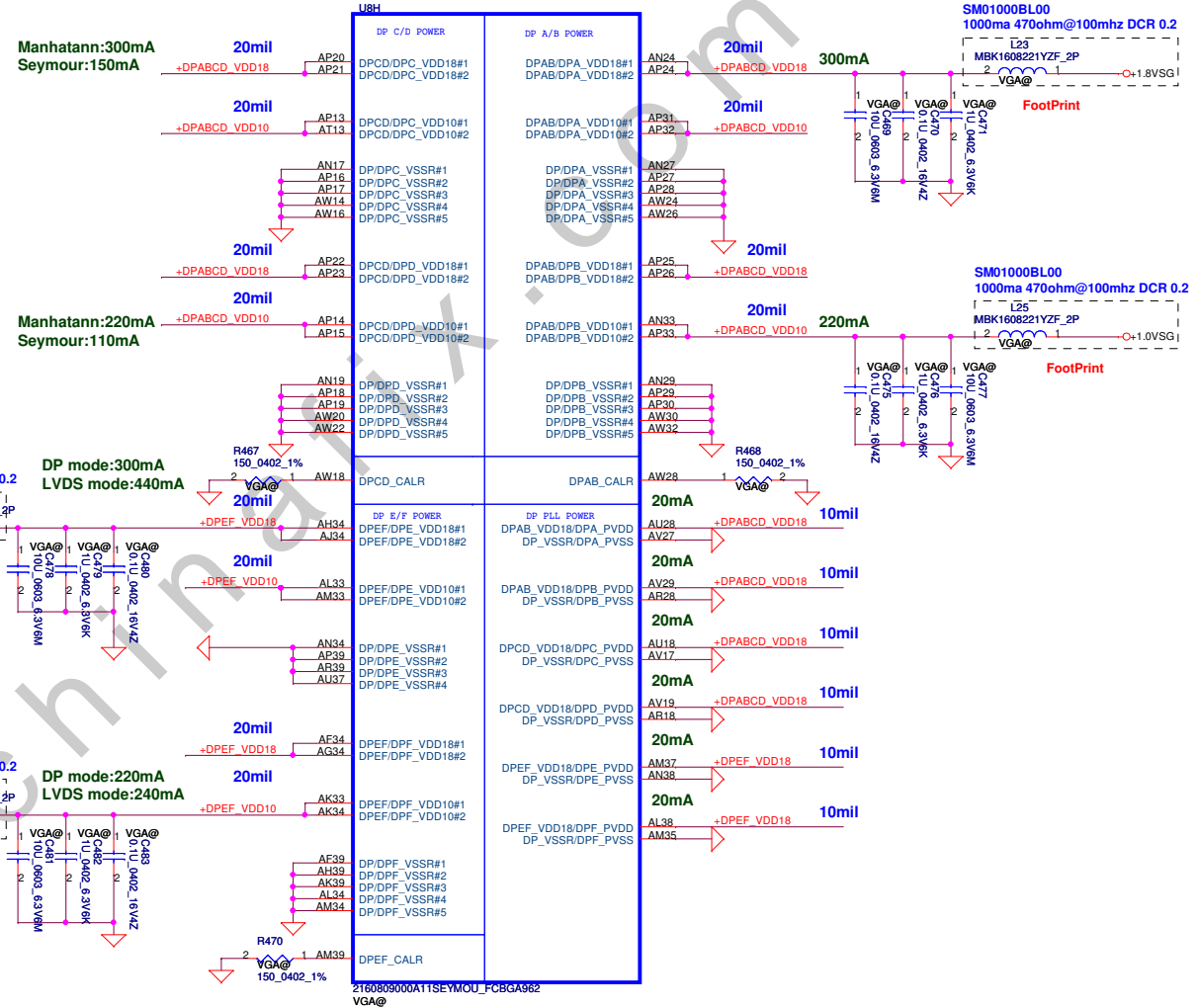
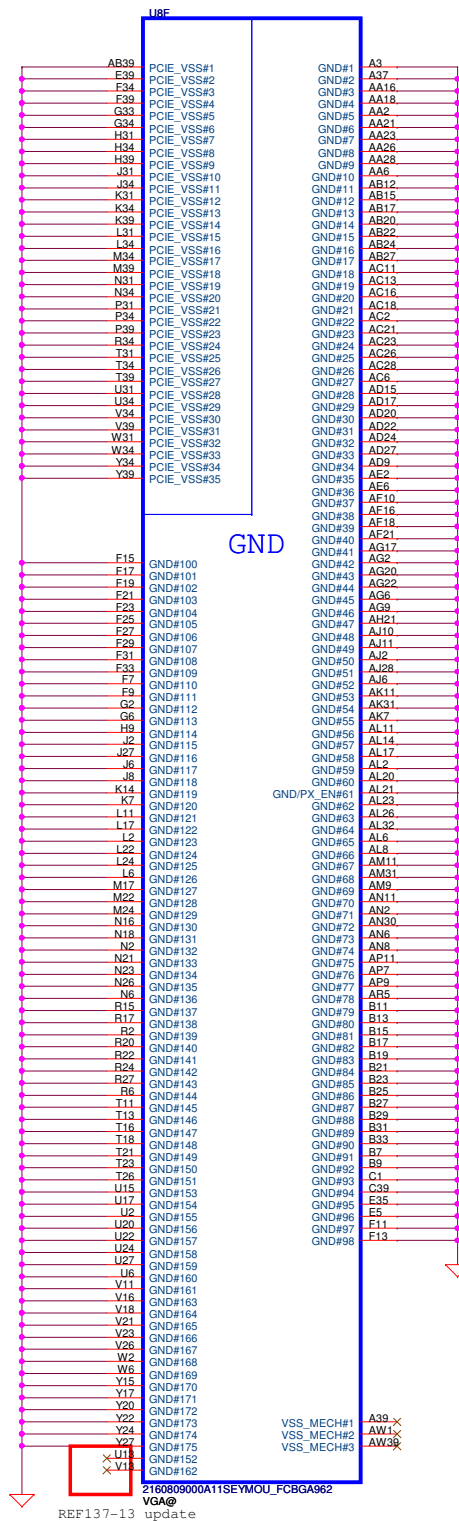




DPA_VDD18,DPA_PVDD,DPB_VDD18,DPB_PVDD
can combian to DPAB_VDD18
DPC_VDD18,DPC_PVDD,DPD_VDD18,DPD_PVDD
can combian to DPCD_VDD18
(DPD_VDD18,DPD_PVDD not applicable on Robson/Park)
DPE_VDD18,DPE_PVDD,DPF_VDD18,DPF_PVDD
can combian to DPEF_VDD18

DPx-VSSR,DPx_PVSS can combian to DP_VSSR
(Manhattan should have individual GND)
where x is A,B,C,D,E,F

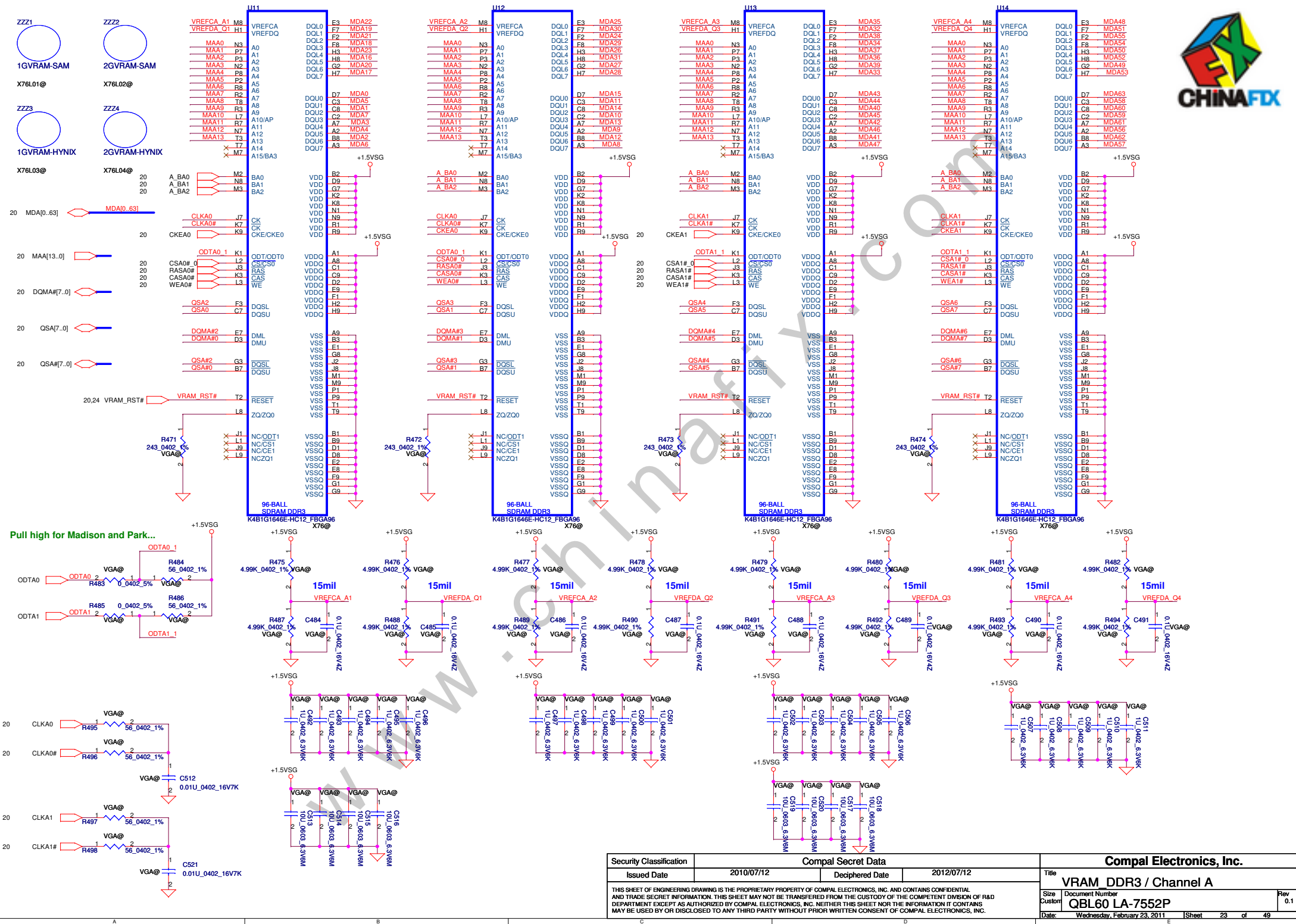
Seymour/Whistler :
DPA_VDD10,DPB_VDD10
can combian to DPAB_VDD10
DPC_VDD10,DPD_VDD10
can combian to DPCD_VDD10
DPE_VDD10,DPD_VDD10
can combian to DPEF_VDD10



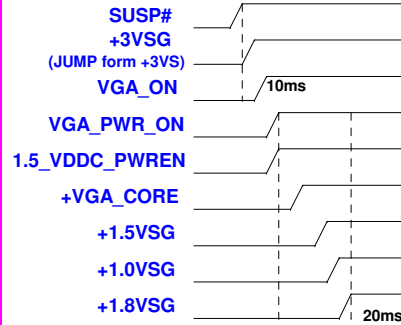
Park/Madison :AL21left NC

Seymour/Whistler:
AL21:PX_EN
use to control discreate GPU regulators
for power express BACO mode
Support BACO:
output High3.3V:turn off regulators (BACO mode on)
output Low0V:turn on regulators (BACO mode off)
need PD resistor
No support BACO:
left NC

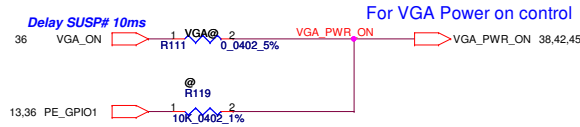
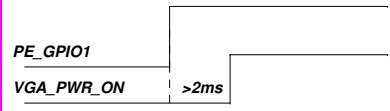
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Power Sequence of Whistler and Seymour



For PX sequence, >2mS delay is required between PE_GPIO1 and VGA_PWR_ON

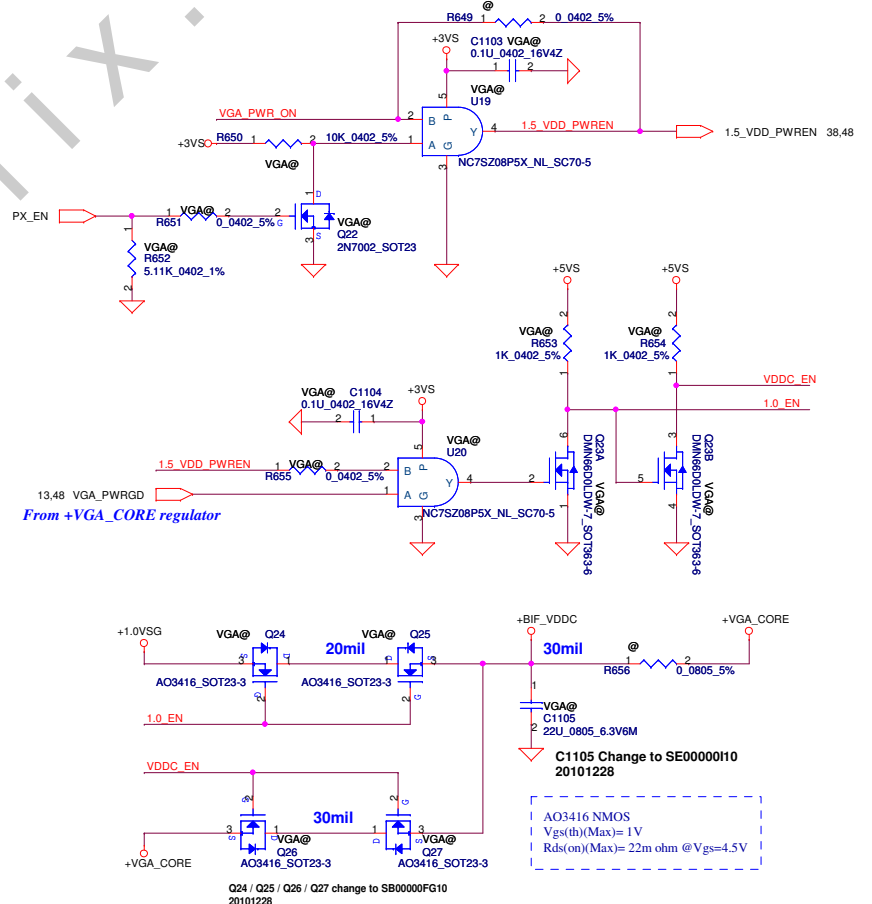


VGA Muxless with BACO Status Mapping table

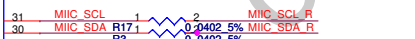
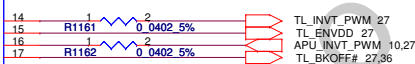
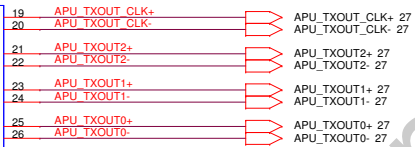
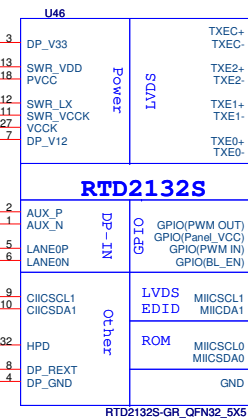
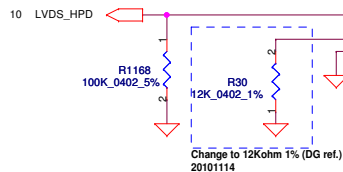
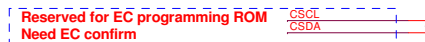
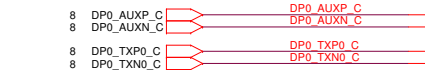
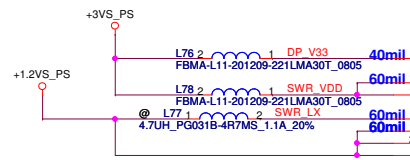
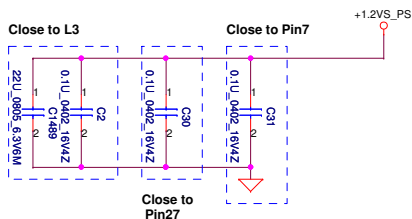
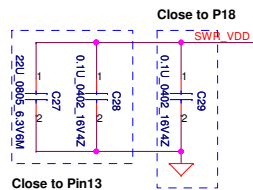
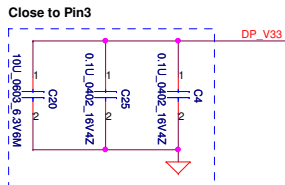
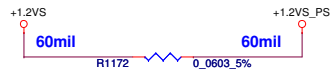
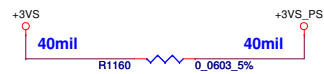
	Normal mode	BACO mode
PX_EN	0	1
1.5_VDDC_PWREN	1	0
VDDC_EN	1	0
1.0_EN	0	1
+3.3VSG	ON	ON
+1.8VSG	ON	ON
+1.0VSG	ON	ON
+VGA_CORE	ON	OFF
+1.5VSG	ON	OFF
+BIF_VDDC	+VGA_CORE	+1.0VSG

VGA Power Enable Signal Mapping table

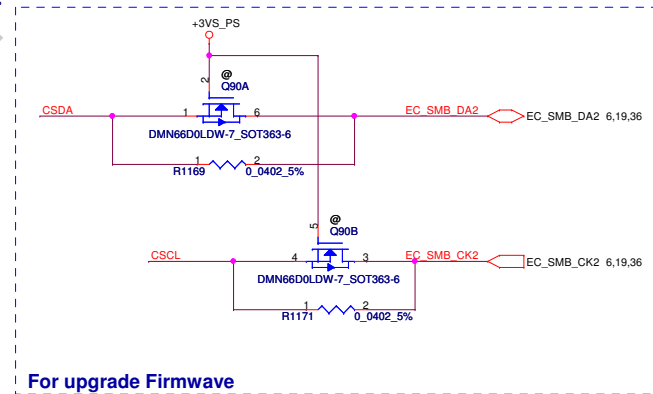
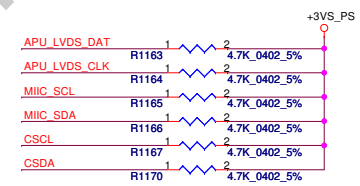
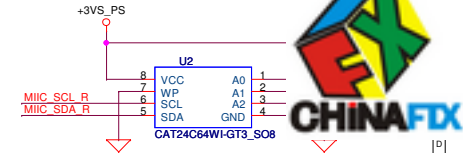
VGA_PWR_ON source signal	Whistler
+3.3VSG	SUSP#
+1.8VSG	VGA_PWR_ON
+1.0VSG	VGA_PWR_ON
+VDDCI	Combine with +VGA_CORE
+VGA_CORE	1.5_VDDC_PWREN
+1.5VSG	1.5_VDDC_PWREN



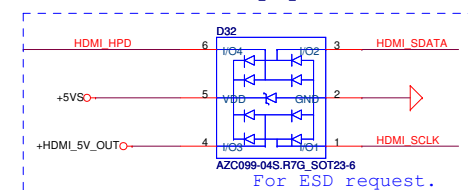
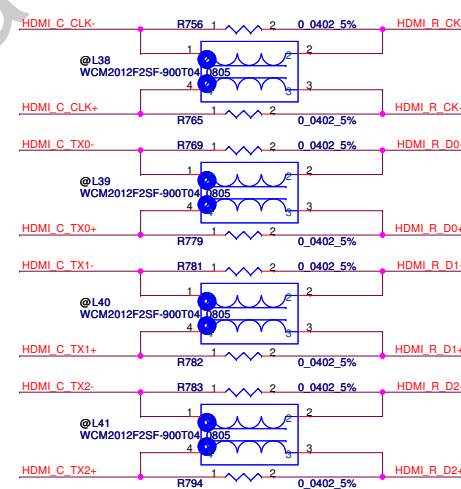
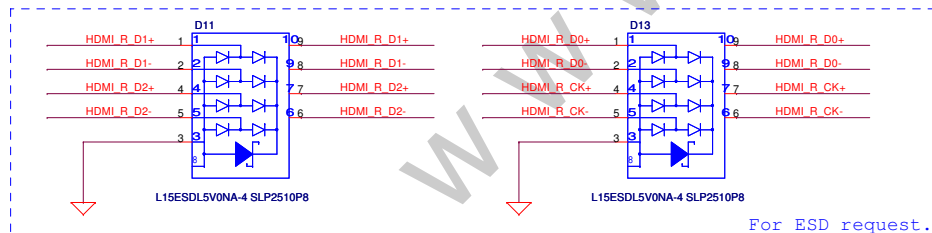
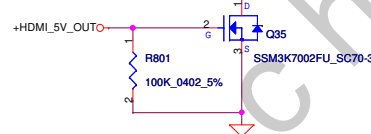
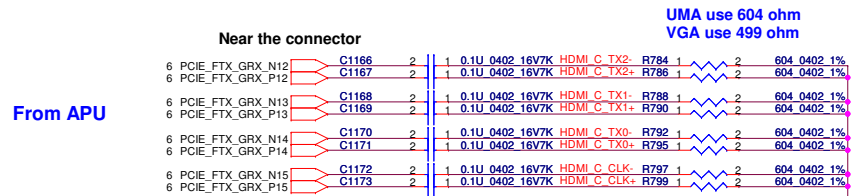
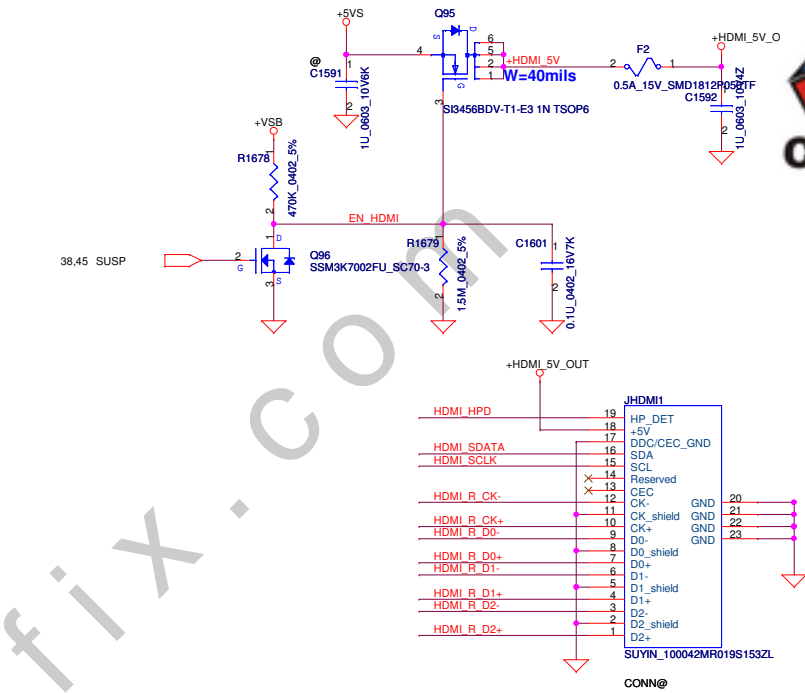
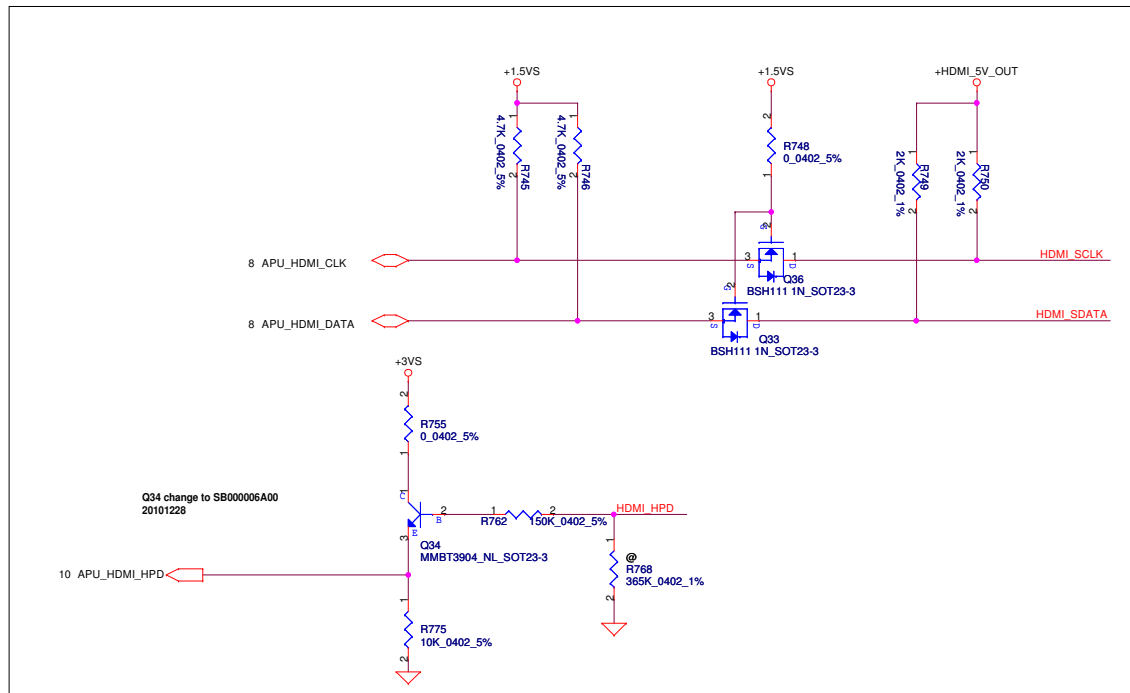
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Issued Date				2010/08/04				Title			
Deciphered Date				2010/08/04				VGA power sequence and BACO			
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				QBL60 LA-7552P				Rev			
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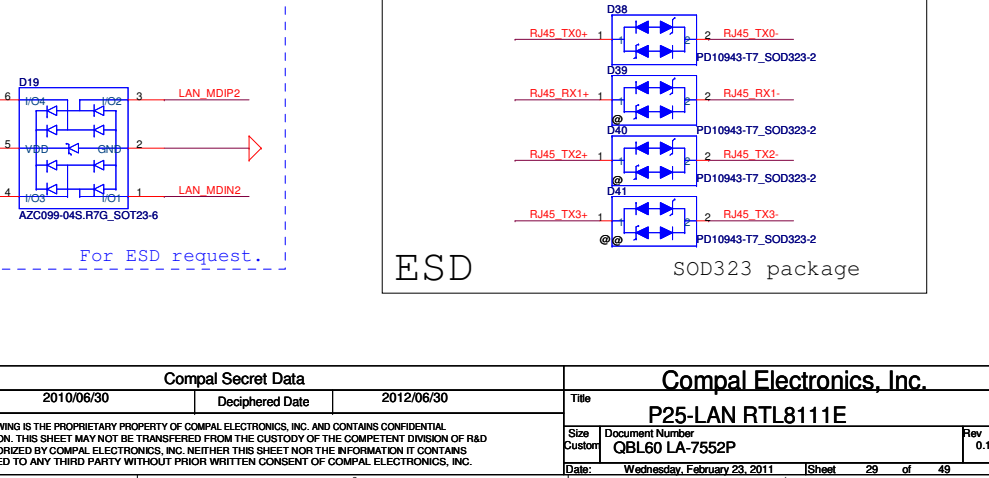
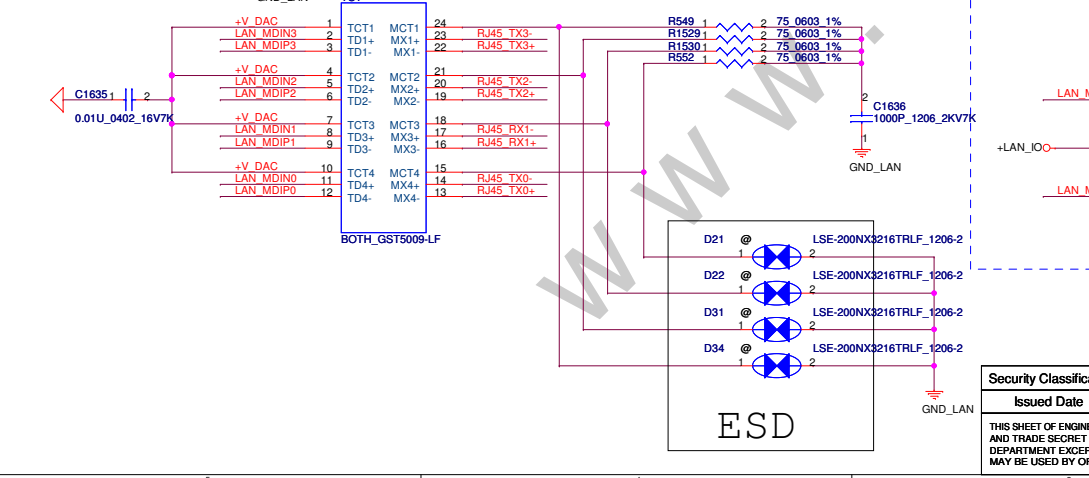
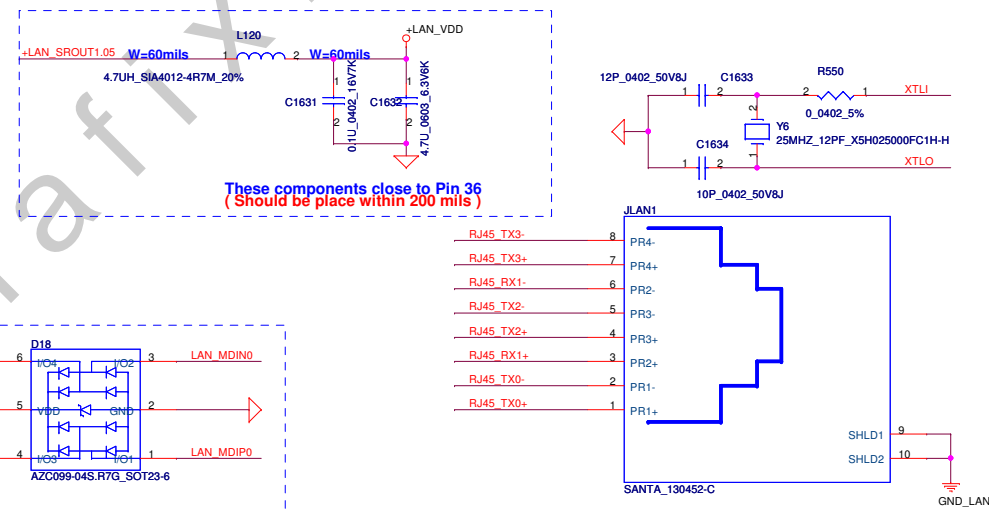
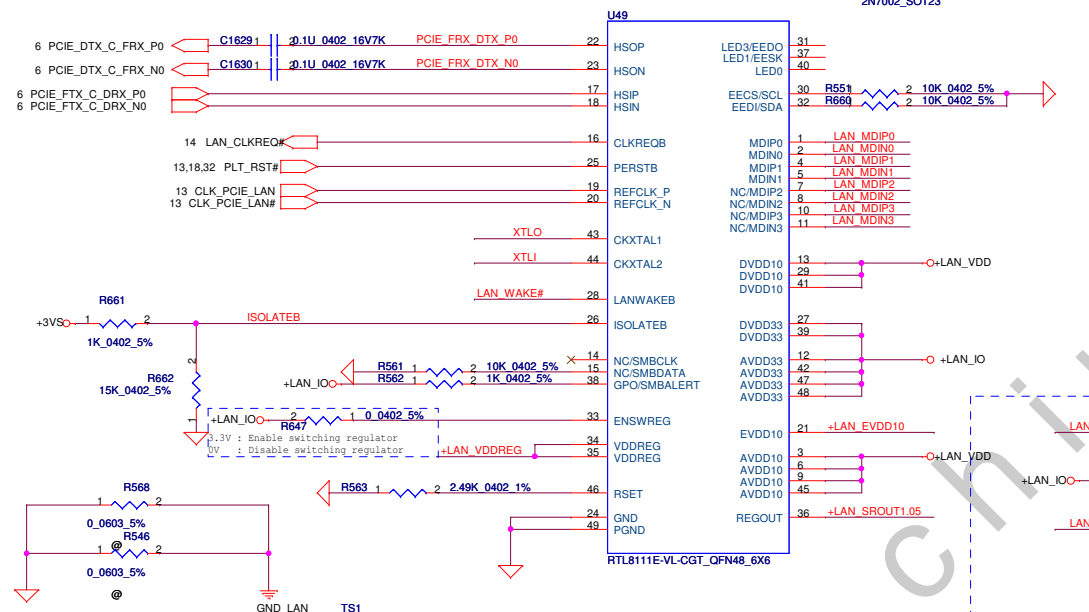
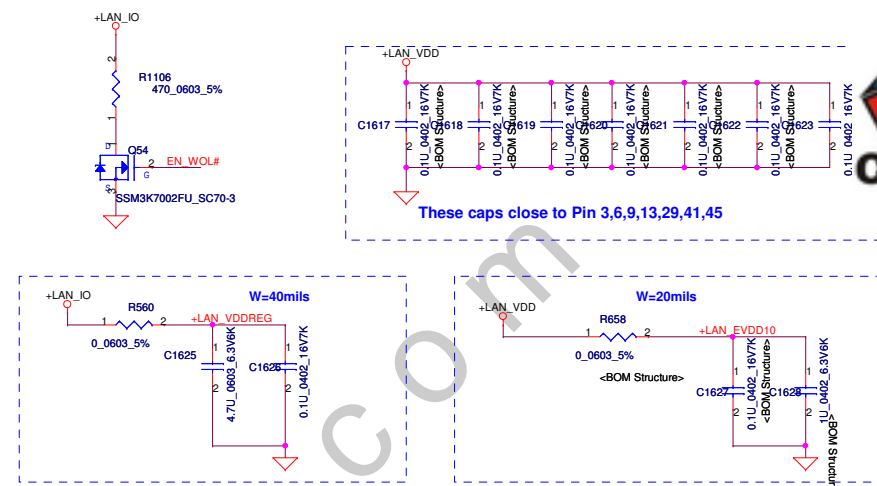
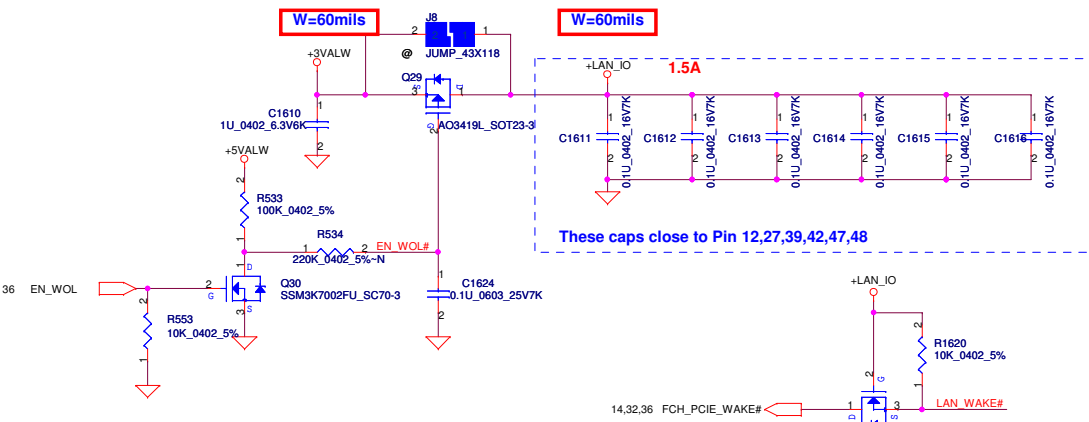
EEROM



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				Size	Document Number	Rev
				Custom	QBL60 LA-7552P	0.1
				Date:	Wednesday, February 23, 2011	Sheet 26 of 49

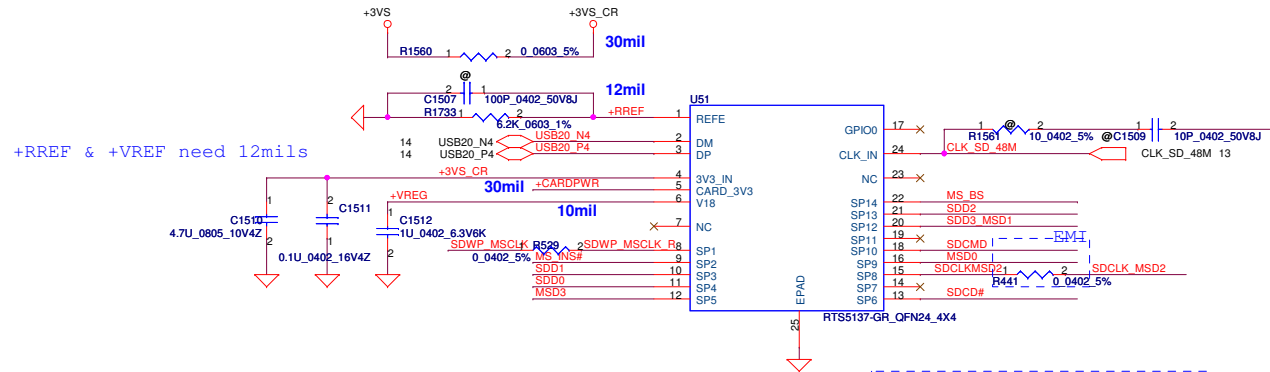


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				Size	Document Number
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				Date	Wednesday, February 23, 2011
				Sheet	28 of 49
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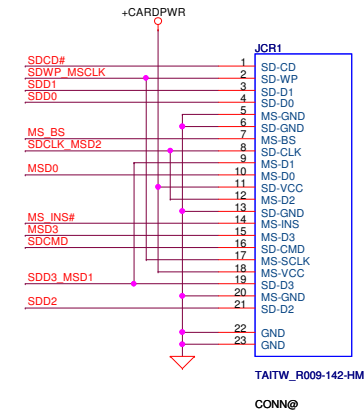
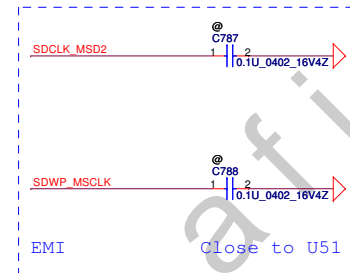
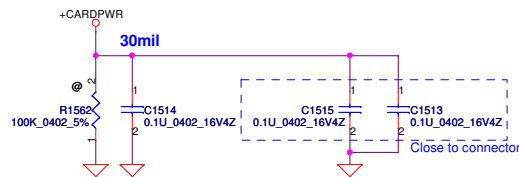


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Card Reader RTS5137 (only SD/MMC/MS function)



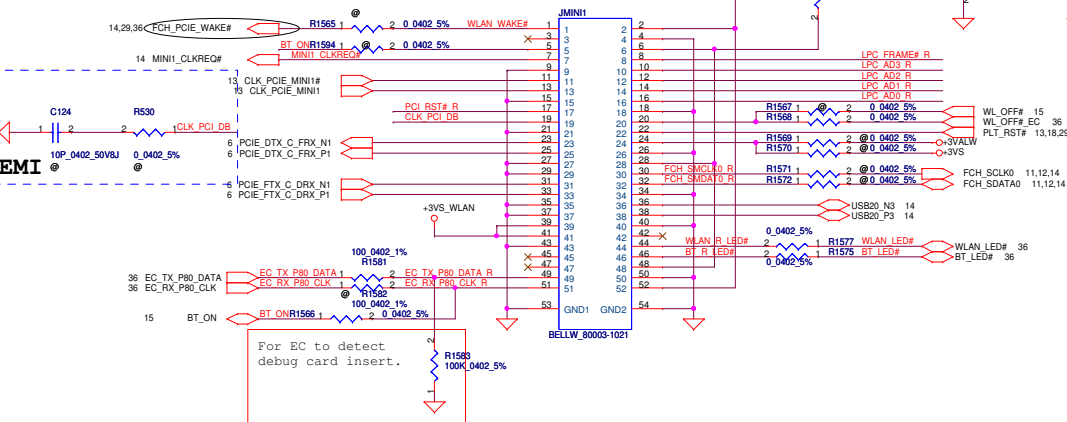
Card Reader Connector



Mini-Express Card for WLAN/WiMAX(Half)



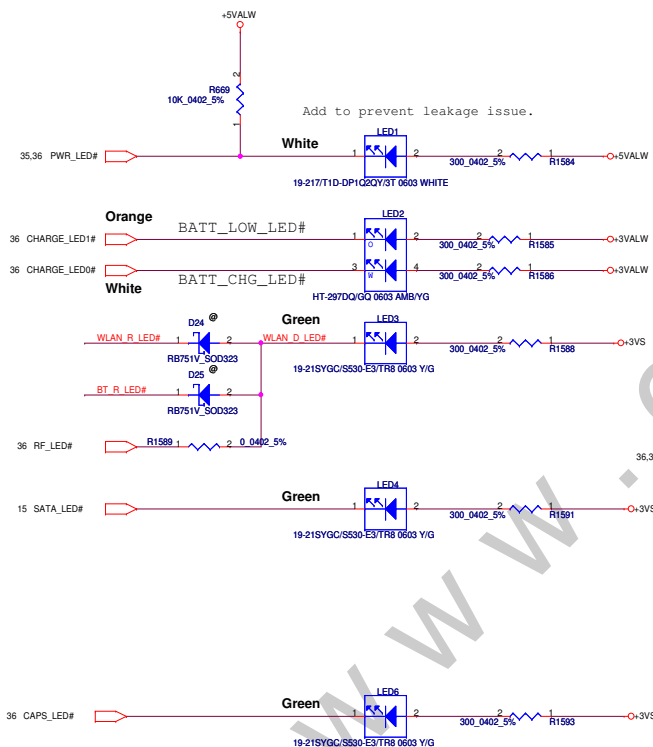
Mini-Express Card(WLAN/WiMAX)



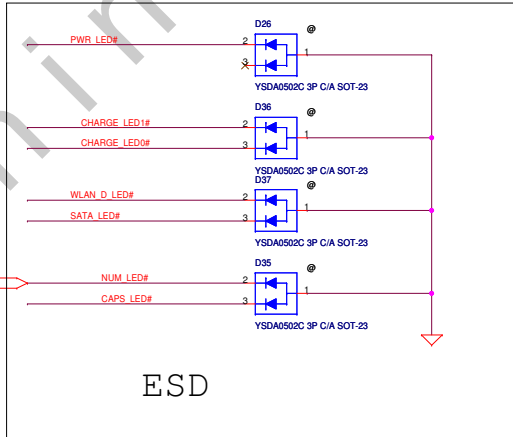
Reserve for SW mini-pcie debug card.
Series resistors closed to KBC side.

LPC_FRAME# R	R1573	1	2	0.0402_5%	LPC_FRAME#	LPC_FRAME#	13,36
LPC_AD3 R	R1574	1	2	0.0402_5%	LPC_AD3	LPC_AD3	13,36
LPC_AD2 R	R1575	1	2	0.0402_5%	LPC_AD2	LPC_AD2	13,36
LPC_AD1 R	R1576	1	2	0.0402_5%	LPC_AD1	LPC_AD1	13,36
LPC_AD0 R	R1577	1	2	0.0402_5%	LPC_AD0	LPC_AD0	13,36
PCI_RST# R	R1578	1	2	0.0402_5%	PLT_RST#	PLT_RST#	13
CLK_PCI_DB	R1579	1	2	0.0402_5%	CLK_PCI_DB	CLK_PCI_DB	13

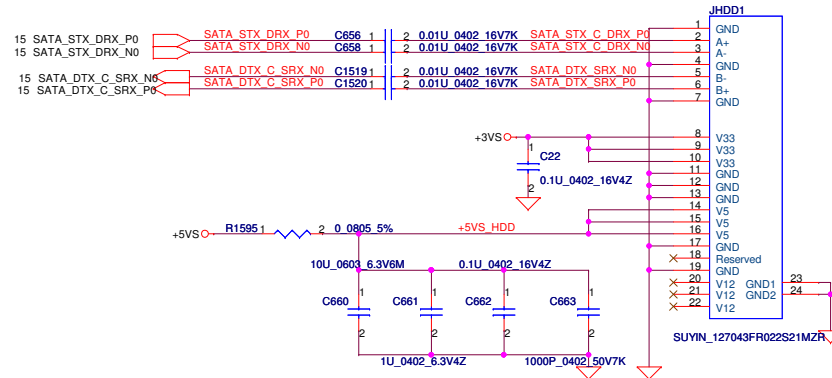
LED



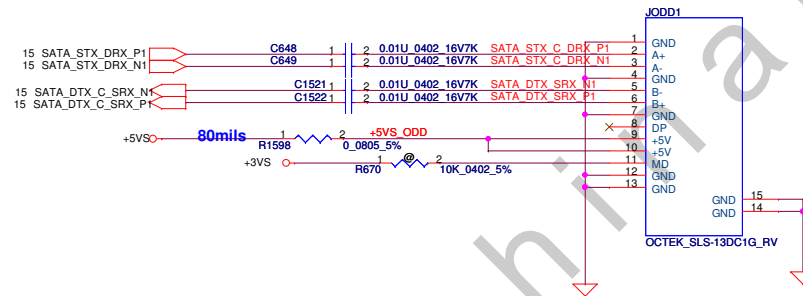
ESD



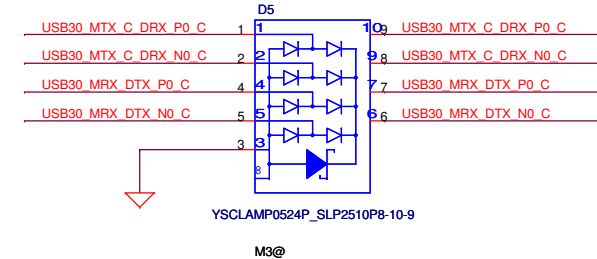
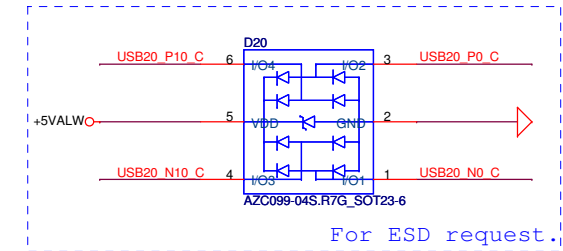
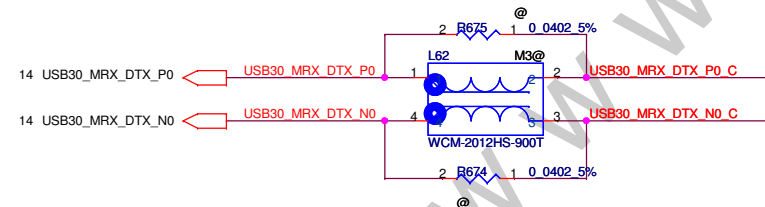
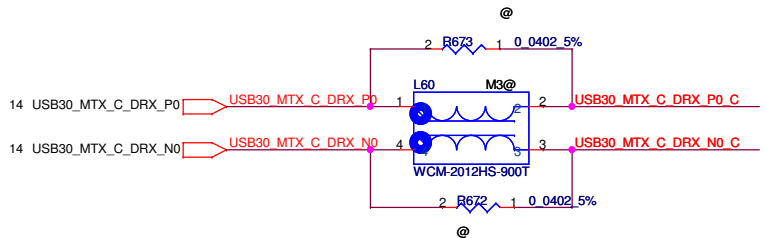
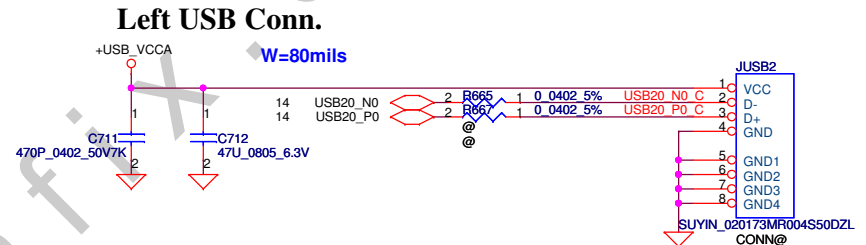
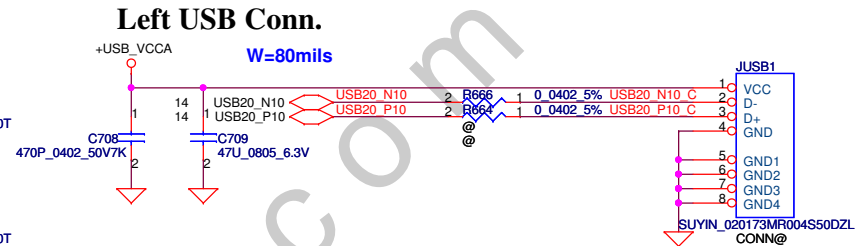
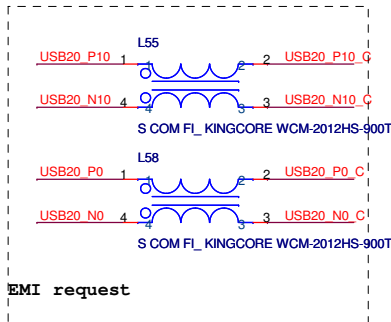
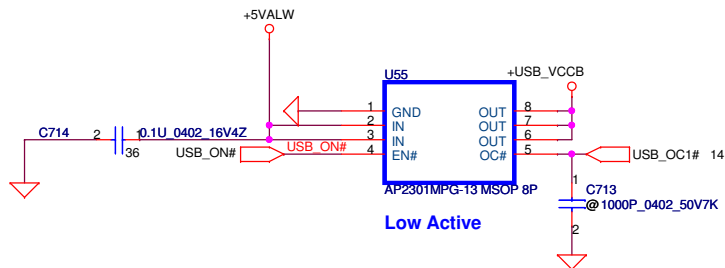
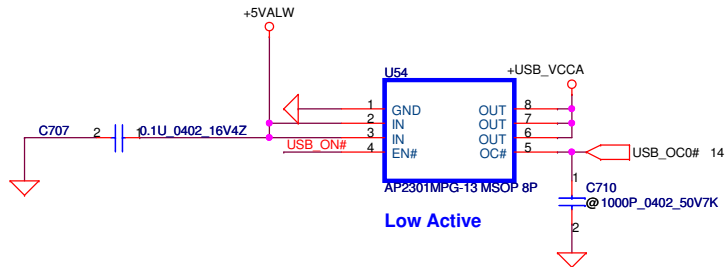
SATA HDD Conn.



SATA ODD FFC Conn.

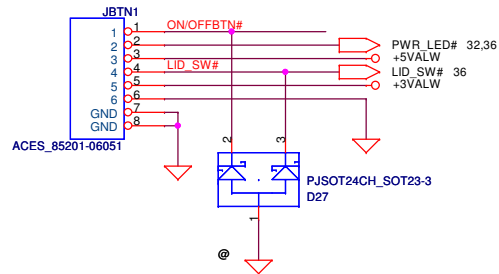
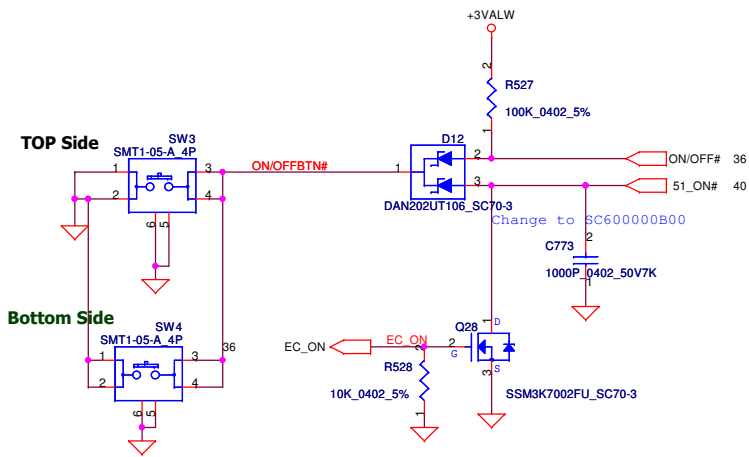


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								Document Number			
								QBL60 LA-7552P			
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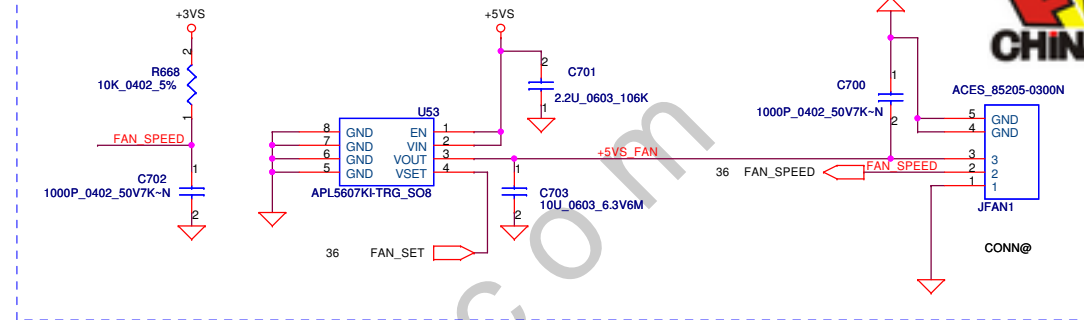


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Size	Custom	Document Number	QBL60 LA-7552P	Rev	0.1
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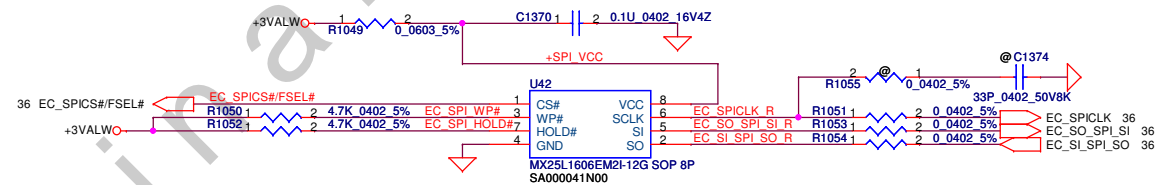
ON/OFF switch **Power Button**



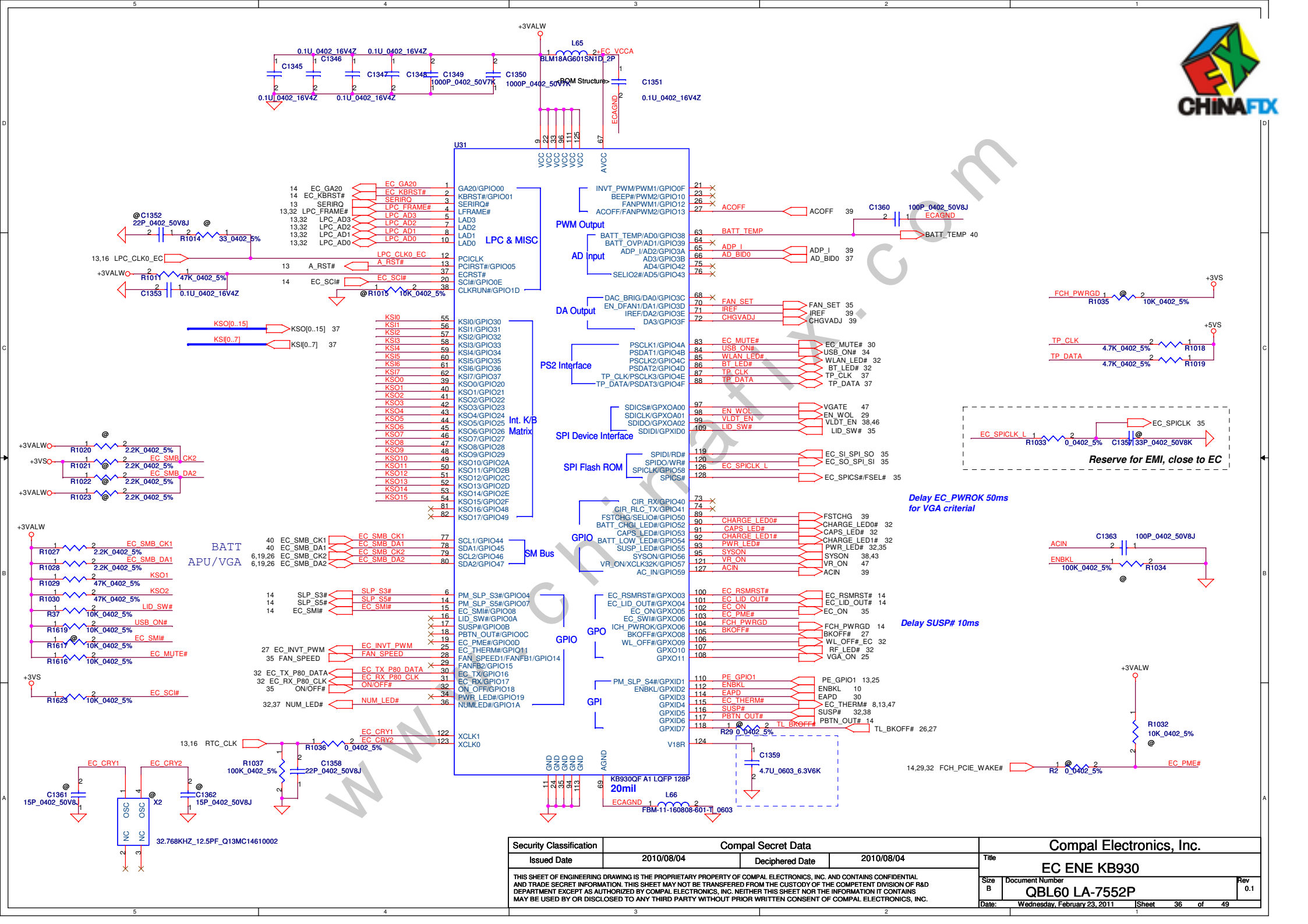
Fan Control Circuit



EC BIOS ROM



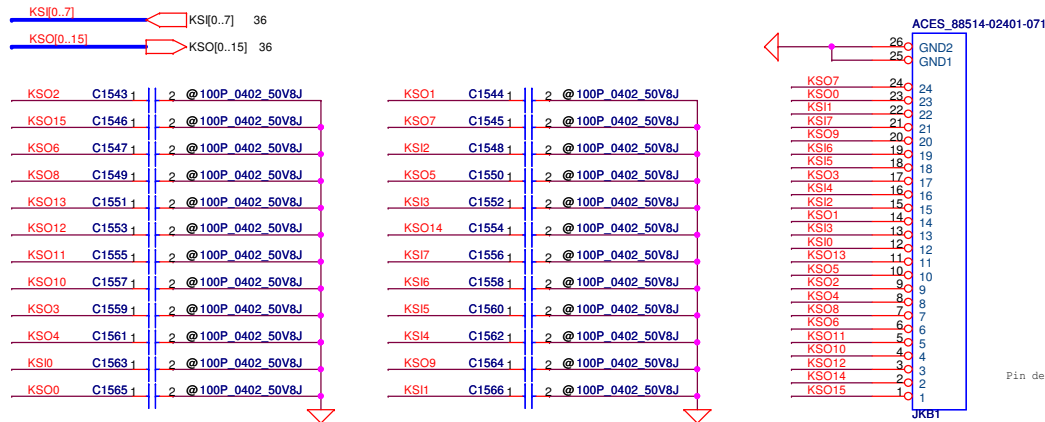
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The schematic diagram illustrates the internal circuitry of the EC ENE KB930 system. At the core is the LPC1114 microcontroller (U31), which is interfaced with several key components:

- Memory:** Includes a 20Mbit SPI Flash ROM (KB930QF A1 LQFP 128P) and a 128Kbit SPI Flash ROM (FBM-11-160808-601-T1 0603).
- Power Management:** Features a BATT APU/VGA section with various capacitors (C1352, C1353, C1354, C1355, C1356, C1357, C1358, C1359) and resistors (R1014, R1015, R1020, R1021, R1022, R1023, R1027, R1028, R1029, R1030, R1032, R1033, R1034, R1035, R1036, R1037, R1038, R1039, R1040, R1041, R1042, R1043, R1044, R1045, R1046, R1047, R1048, R1049, R1050, R1051, R1052, R1053, R1054, R1055, R1056, R1057, R1058, R1059, R1060, R1061, R1062, R1063, R1064, R1065, R1066, R1067, R1068, R1069, R1070, R1071, R1072, R1073, R1074, R1075, R1076, R1077, R1078, R1079, R1080, R1081, R1082, R1083, R1084, R1085, R1086, R1087, R1088, R1089, R1090, R1091, R1092, R1093, R1094, R1095, R1096, R1097, R1098, R1099, R1100, R1101, R1102, R1103, R1104, R1105, R1106, R1107, R1108, R1109, R1110, R1111, R1112, R1113, R1114, R1115, R1116, R1117, R1118, R1119, R1120, R1121, R1122, R1123, R1124, R1125, R1126, R1127, R1128, R1129, R1130, R1131, R1132, R1133, R1134, R1135, R1136, R1137, R1138, R1139, R1140, R1141, R1142, R1143, R1144, R1145, R1146, R1147, R1148, R1149, R1150, R1151, R1152, R1153, R1154, R1155, R1156, R1157, R1158, R1159, R1160, R1161, R1162, R1163, R1164, R1165, R1166, R1167, R1168, R1169, R1170, R1171, R1172, R1173, R1174, R1175, R1176, R1177, R1178, R1179, R1180, R1181, R1182, R1183, R1184, R1185, R1186, R1187, R1188, R1189, R1190, R1191, R1192, R1193, R1194, R1195, R1196, R1197, R1198, R1199, R1200, R1201, R1202, R1203, R1204, R1205, R1206, R1207, R1208, R1209, R1210, R1211, R1212, R1213, R1214, R1215, R1216, R1217, R1218, R1219, R1220, R1221, R1222, R1223, R1224, R1225, R1226, R1227, R1228, R1229, R1230, R1231, R1232, R1233, R1234, R1235, R1236, R1237, R1238, R1239, R1240, R1241, R1242, R1243, R1244, R1245, R1246, R1247, R1248, R1249, R1250, R1251, R1252, R1253, R1254, R1255, R1256, R1257, R1258, R1259, R1260, R1261, R1262, R1263, R1264, R1265, R1266, R1267, R1268, R1269, R1270, R1271, R1272, R1273, R1274, R1275, R1276, R1277, R1278, R1279, R1280, R1281, R1282, R1283, R1284, R1285, R1286, R1287, R1288, R1289, R1290, R1291, R1292, R1293, R1294, R1295, R1296, R1297, R1298, R1299, R1300, R1301, R1302, R1303, R1304, R1305, R1306, R1307, R1308, R1309, R1310, R1311, R1312, R1313, R1314, R1315, R1316, R1317, R1318, R1319, R1320, R1321, R1322, R1323, R1324, R1325, R1326, R1327, R1328, R1329, R1330, R1331, R1332, R1333, R1334, R1335, R1336, R1337, R1338, R1339, R1340, R1341, R1342, R1343, R1344, R1345, R1346, R1347, R1348, R1349, R1350, R1351, R1352, R1353, R1354, R1355, R1356, R1357, R1358, R1359, R1360, R1361, R1362, R1363, R1364, R1365, R1366, R1367, R1368, R1369, R1370, R1371, R1372, R1373, R1374, R1375, R1376, R1377, R1378, R1379, R1380, R1381, R1382, R1383, R1384, R1385, R1386, R1387, R1388, R1389, R1390, R1391, R1392, R1393, R1394, R1395, R1396, R1397, R1398, R1399, R1400, R1401, R1402, R1403, R1404, R1405, R1406, R1407, R1408, R1409, R1410, R1411, R1412, R1413, R1414, R1415, R1416, R1417, R1418, R1419, R1420, R1421, R1422, R1423, R1424, R1425, R1426, R1427, R1428, R1429, R1430, R1431, R1432, R1433, R1434, R1435, R1436, R1437, R1438, R1439, R1440, R1441, R1442, R1443, R1444, R1445, R1446, R1447, R1448, R1449, R1450, R1451, R1452, R1453, R1454, R1455, R1456, R1457, R1458, R1459, R1460, R1461, R1462, R1463, R1464, R1465, R1466, R1467, R1468, R1469, R1470, R1471, R1472, R1473, R1474, R1475, R1476, R1477, R1478, R1479, R1480, R1481, R1482, R1483, R1484, R1485, R1486, R1487, R1488, R1489, R1490, R1491, R1492, R1493, R1494, R1495, R1496, R1497, R1498, R1499, R1500, R1501, R1502, R1503, R1504, R1505, R1506, R1507, R1508, R1509, R1510, R1511, R1512, R1513, R1514, R1515, R1516, R1517, R1518, R1519, R1520, R1521, R1522, R1523, R1524, R1525, R1526, R1527, R1528, R1529, R1530, R1531, R1532, R1533, R1534, R1535, R1536, R1537, R1538, R1539, R1540, R1541, R1542, R1543, R1544, R1545, R1546, R1547, R1548, R1549, R1550, R1551, R1552, R1553, R1554, R1555, R1556, R1557, R1558, R1559, R1560, R1561, R1562, R1563, R1564, R1565, R1566, R1567, R1568, R1569, R1570, R1571, R1572, R1573, R1574, R1575, R1576, R1577, R1578, R1579, R1580, R1581, R1582, R1583, R1584, R1585, R1586, R1587, R1588, R1589, R1590, R1591, R1592, R1593, R1594, R1595, R1596, R1597, R1598, R1599, R1600, R1601, R1602, R1603, R1604, R1605, R1606, R1607, R1608, R1609, R1610, R1611, R1612, R1613, R1614, R1615, R1616, R1617, R1618, R1619, R1620, R1621, R1622, R1623, R1624, R1625, R1626, R1627, R1628, R1629, R1630, R1631, R1632, R1633, R1634, R1635, R1636, R1637, R1638, R1639, R1640, R1641, R1642, R1643, R1644, R1645, R1646, R1647, R1648, R1649, R1650, R1651, R1652, R1653, R1654, R1655, R1656, R1657, R1658, R1659, R1660, R1661, R1662, R1663,

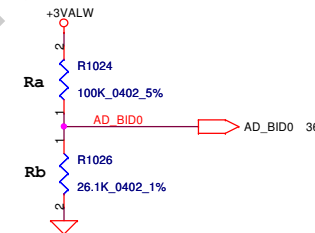
INT_KBD Conn.



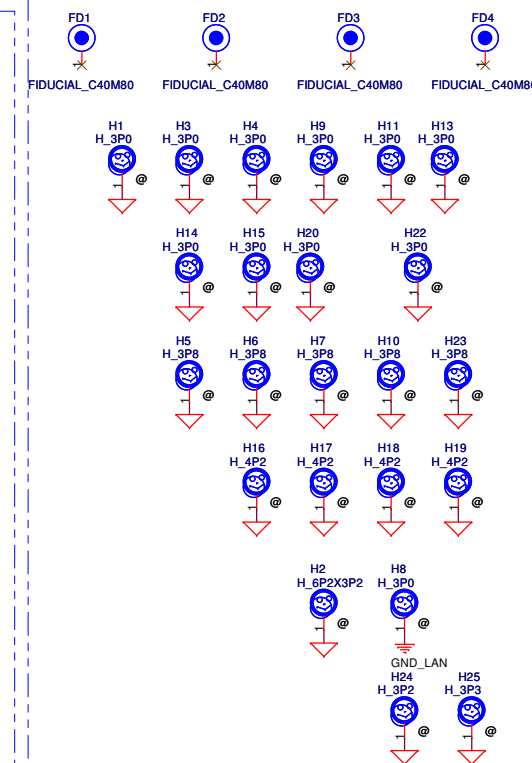
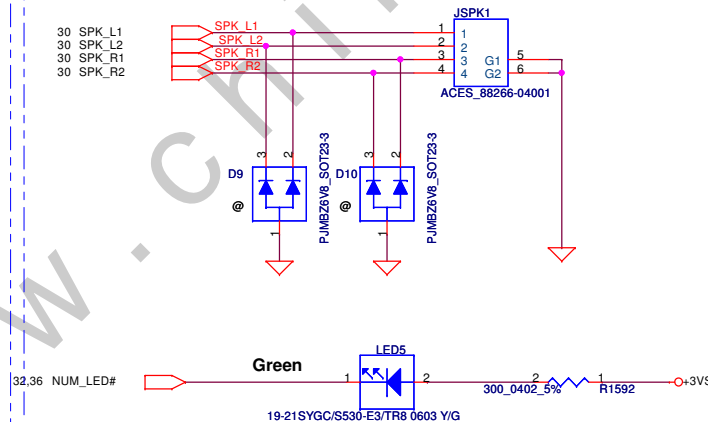
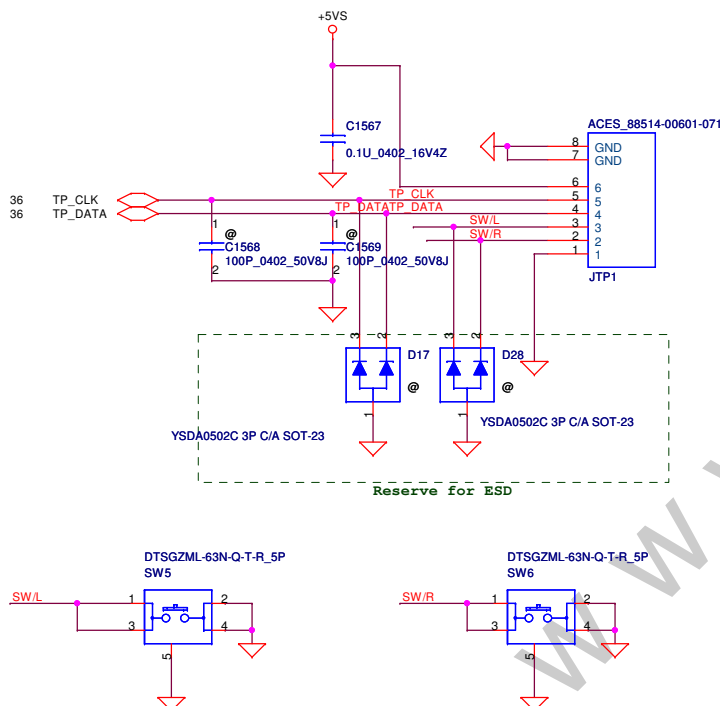
ID	BRD ID	Ra	Rb	Vab
0	R01 SR	100K	26.1K	0.683V
1	R02 ER	100K	34.8K	0.851V
2	R03 PR	100K	46.4K	1.045V
3	R10 MP	100K	56.2K	1.187V



Analog Board ID definition

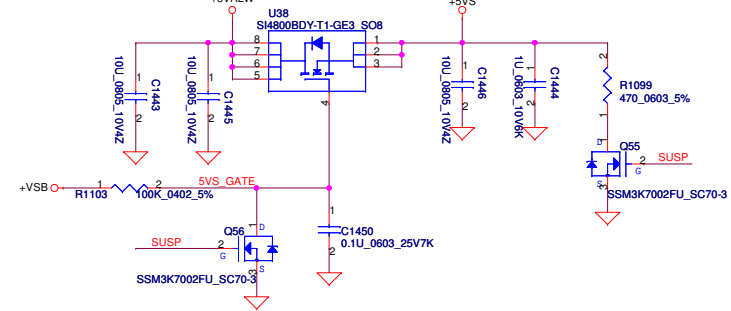


To TP/B Conn.

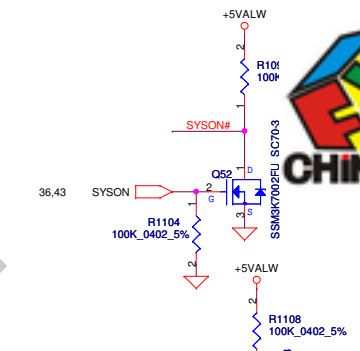
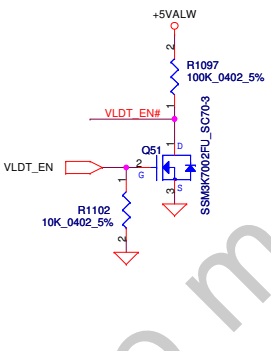
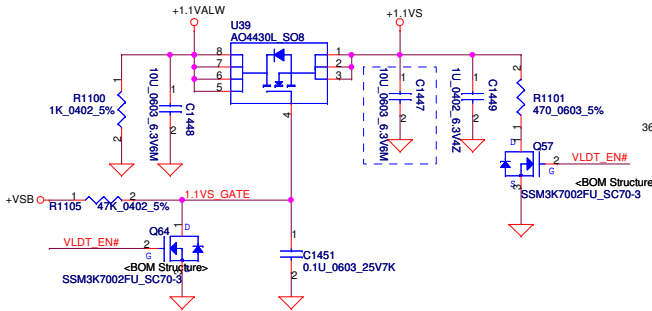


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				Date: Wednesday, February 23, 2011	Sheet 37 of 49

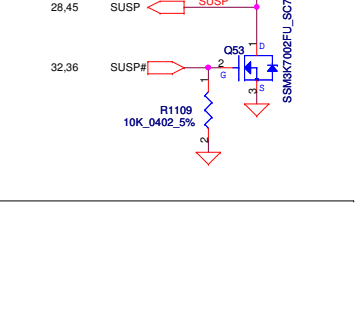
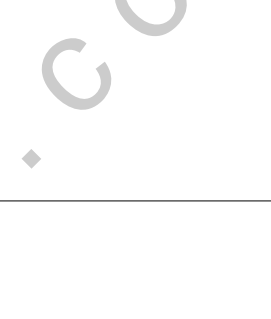
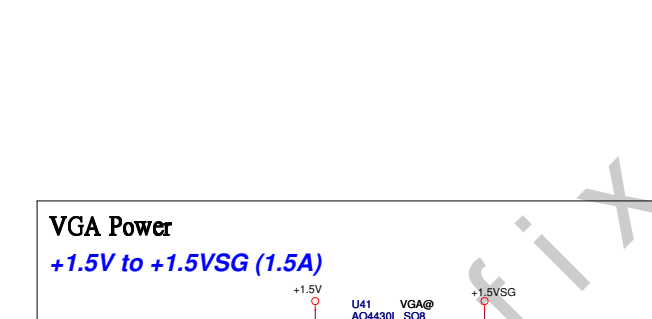
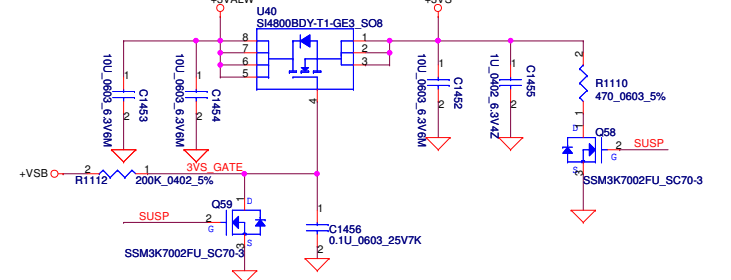
+5VALW TO +5VS (5A)



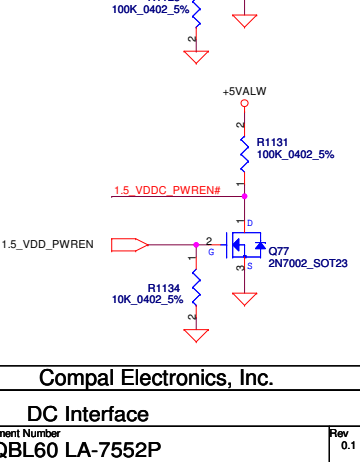
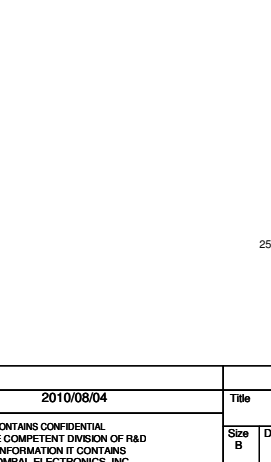
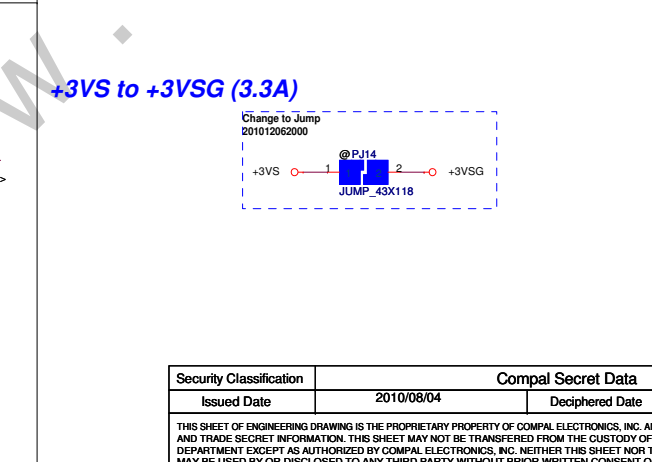
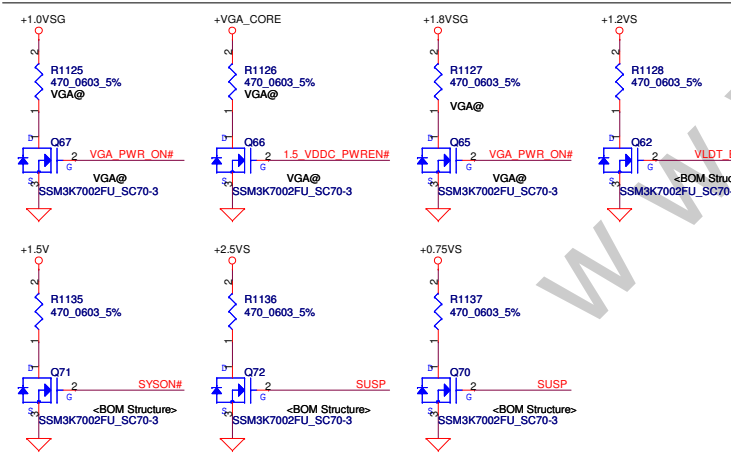
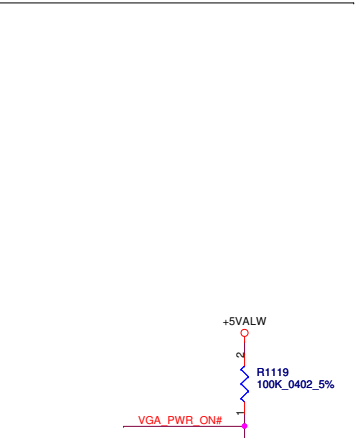
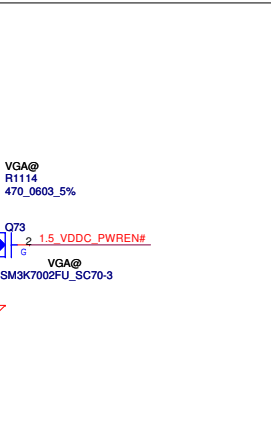
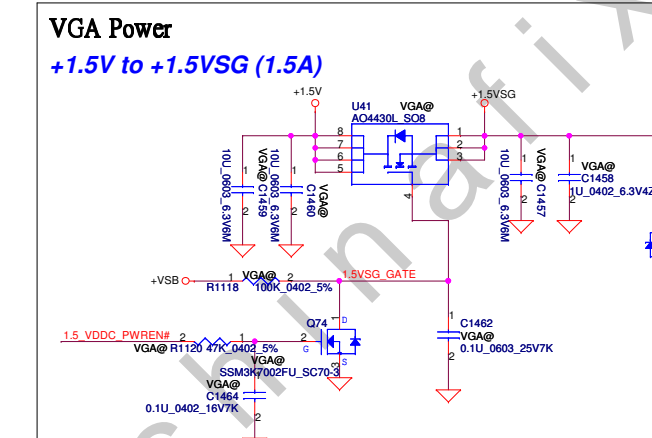
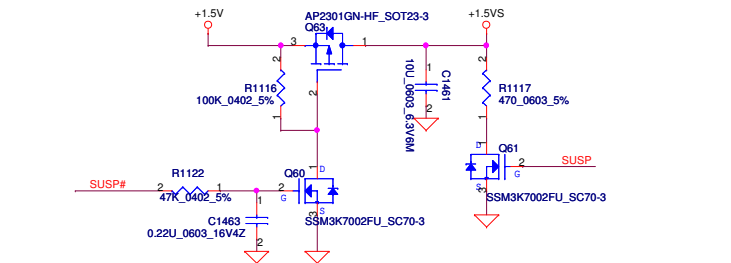
+1.1VALW TO +1.1VS (1.1A)



+3VALW TO +3VS (3.3A)

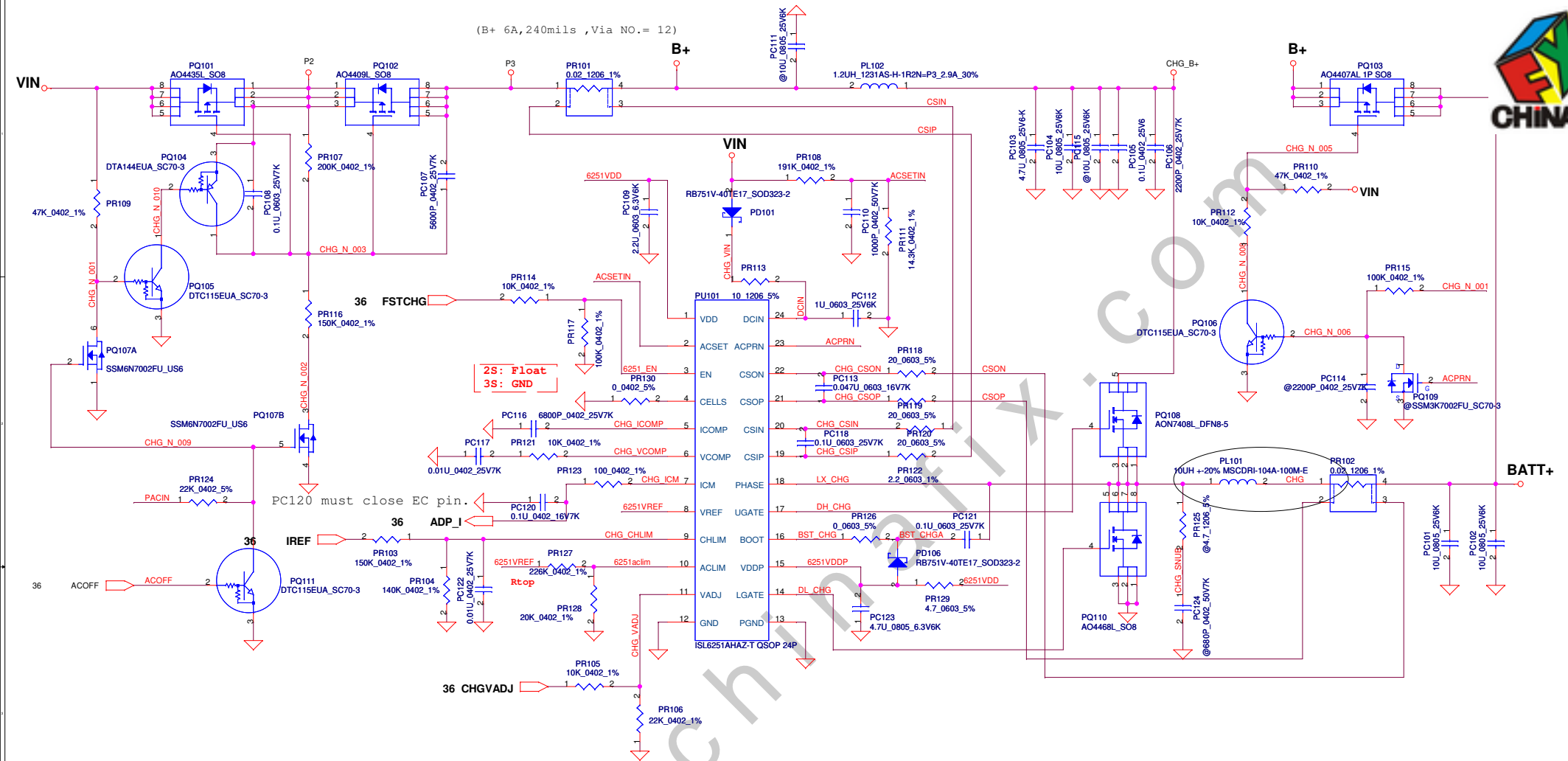


+1.5V TO +1.5VS (1.5A)



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(B+ 6A,240mils ,Via NO.= 12)



CP= 85%*I_{ada};

I_{ada}=0~4.737A (90W); CP=4.03A; where R_{acdet}=0.020ohm, where R_{top}=12.4K
90W for Dis: R_{top}=SD00000AJ80
I_{ada}=0~3.421A (65W); CP=2.91A; where R_{acdet}=0.020ohm, where R_{top}=226K
65W for UMA: R_{top}=SD034226380
Astro2010_01_15 need confirm P/N

CP mode

V_{aclim}=V_{REF}*(R_{bot}//R_{internal}/(R_{top}//R_{internal}+R_{bot}//R_{internal}))
when 90W V_{aclim}=2.39*(20K//152K/(20K//152K+12.4K//152K))=1.44966V
when 65W V_{aclim}=2.39*(20K//152K/(20K//152K+226K//152K))=0.38914V
I_{input}=(1/R_{acdet})*(0.05*V_{aclim}/V_{REF}+0.05)
when 90W, I_{input}=(1/0.02)*(0.05*1.44966/2.39+0.05)=4.02A
when 65W, I_{input}=(1/0.02)*(0.05*0.38914/2.39+0.05)=2.92A

CC=0.25A~3A

I_{REF}=1.016*I_{charge}

I_{REF}=0.254V~3.048V

V_{CHLIM} need over 95mV

CHGVADJ=(V_{cell}-4)/0.10627

V_{cell} CHGVADJ

4V 0V

4.2V 1.882V

Security Classification		Compal Secret Data	
Issued Date	2009/01/23	Deciphered Date	2010/01/23

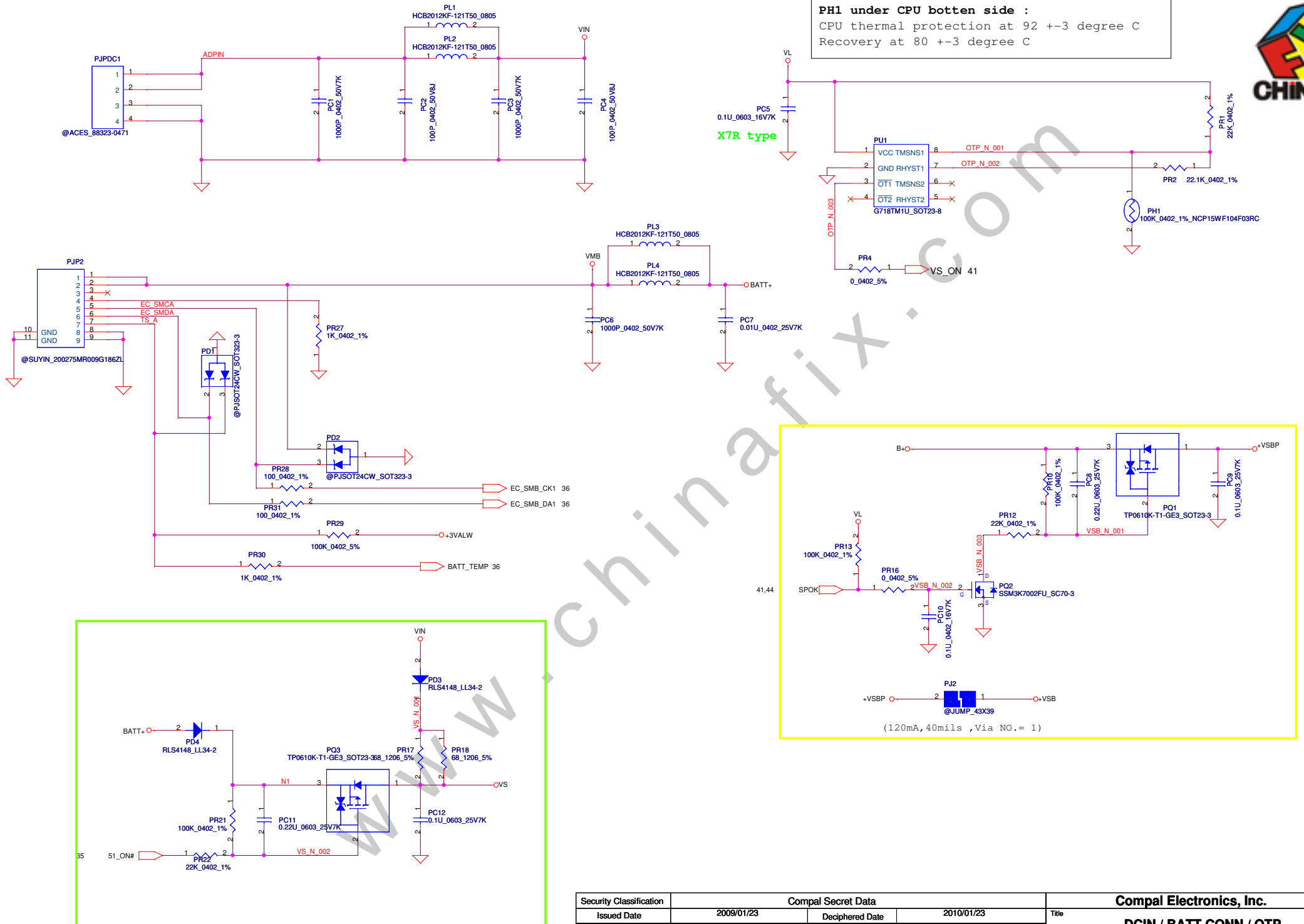
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Compal Electronics, Inc.

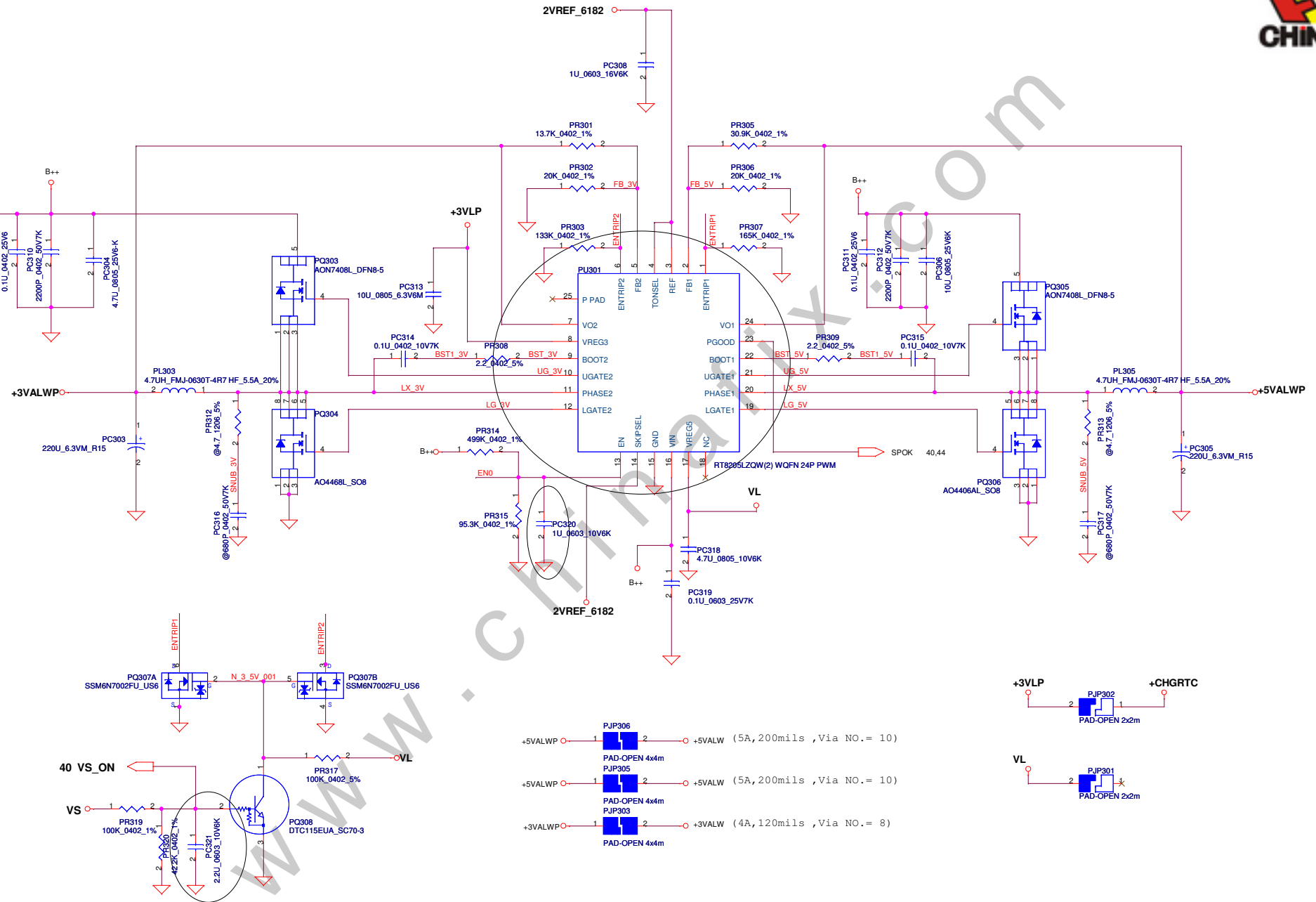
CHARGER

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Date:	Wednesday, February 23, 2011	Sheet 39 of 49

PH1 under CPU bottom side :
CPU thermal protection at 92 \pm 3 degree C
Recovery at 80 \pm 3 degree C



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				Date	Rev
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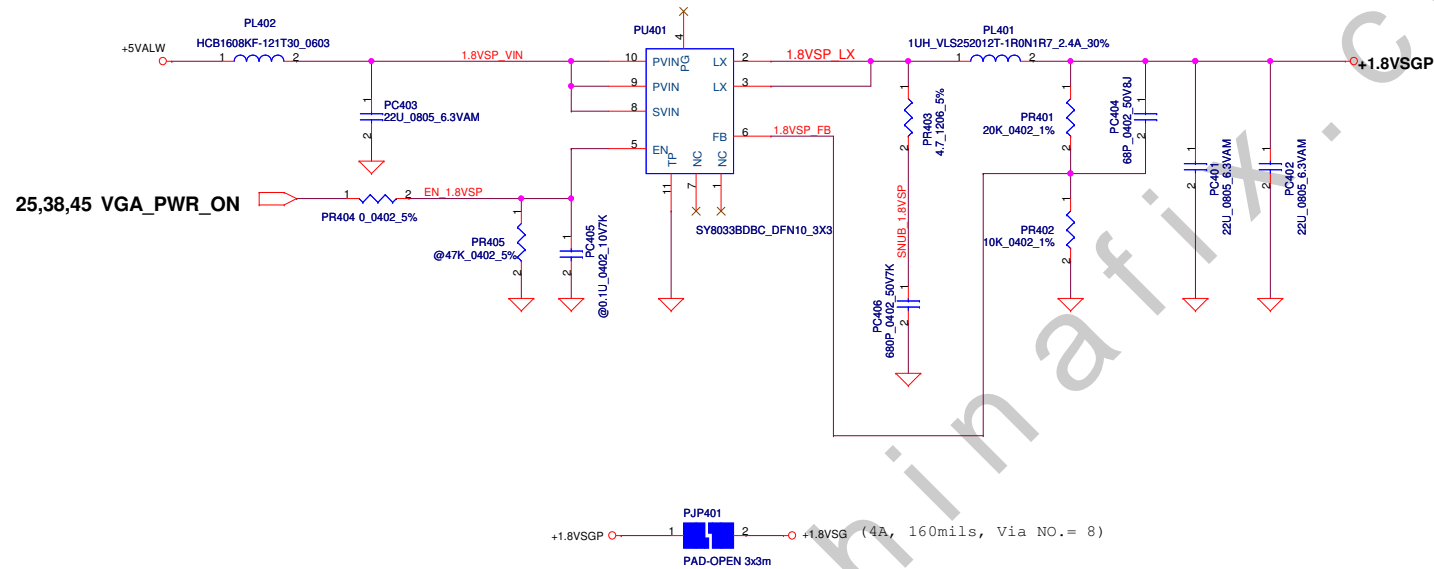
EC:+3VL, reserve PR319, install PR318, PR320 100K
EC:+3VALW, reserve PR318, install PR319, PR320 42.2K

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				Date	Wednesday, February 23, 2011
				Sheet	41 of 49

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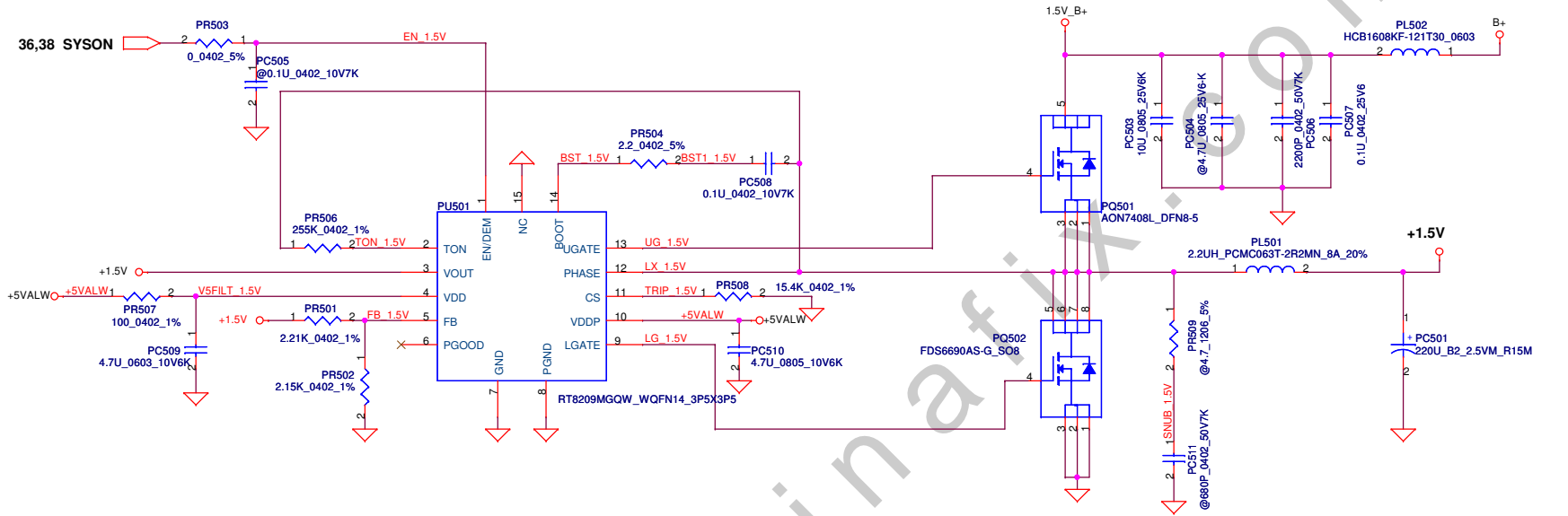
3.3VALWP/5VALWP

Rev 0.1
Date: Wednesday, February 23, 2011



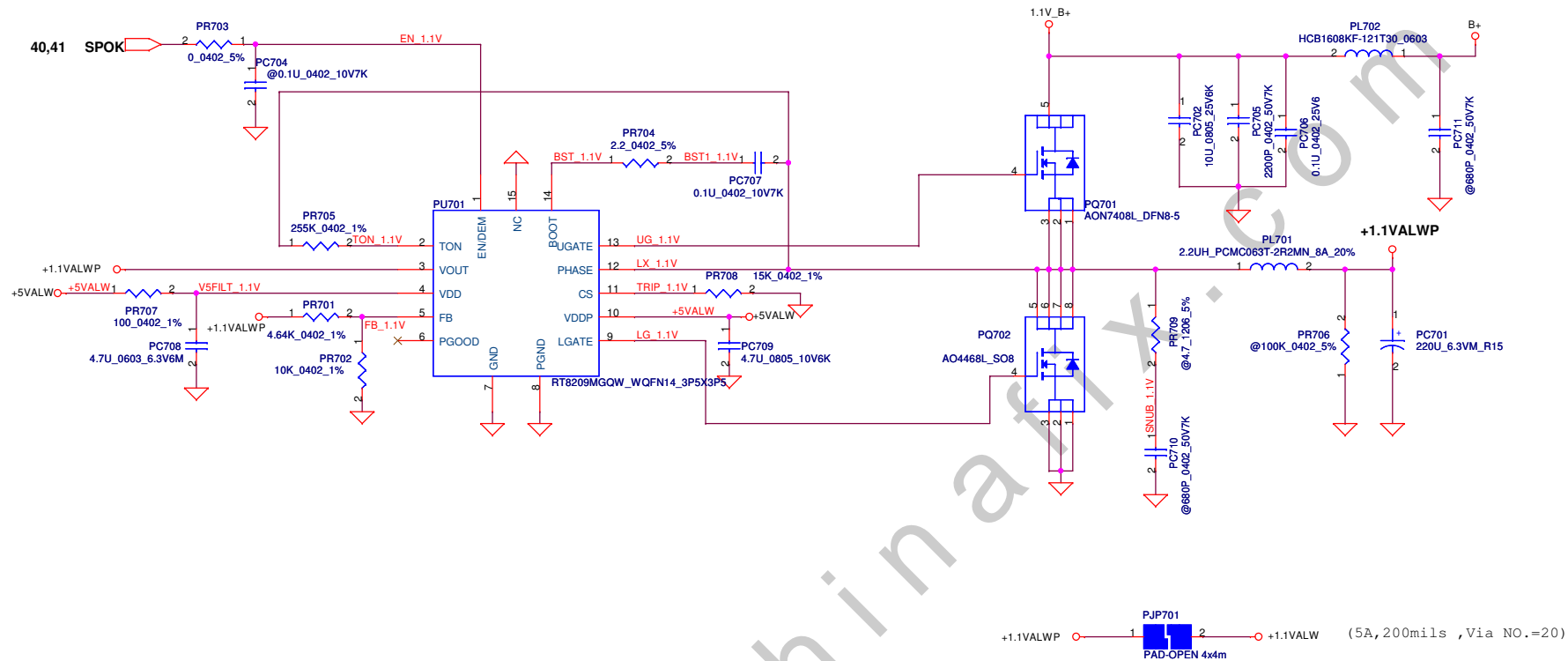
$$\begin{aligned} <V_o=1.8V> \quad V_{FB}=0.6V \\ V_o=V_{FB} * (1+PR401/PR402)=0.6 * (1+20K/10K)=1.8V \end{aligned}$$

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Size	Document Number	NCL61 LA-6321P M/B			Rev
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					0.1

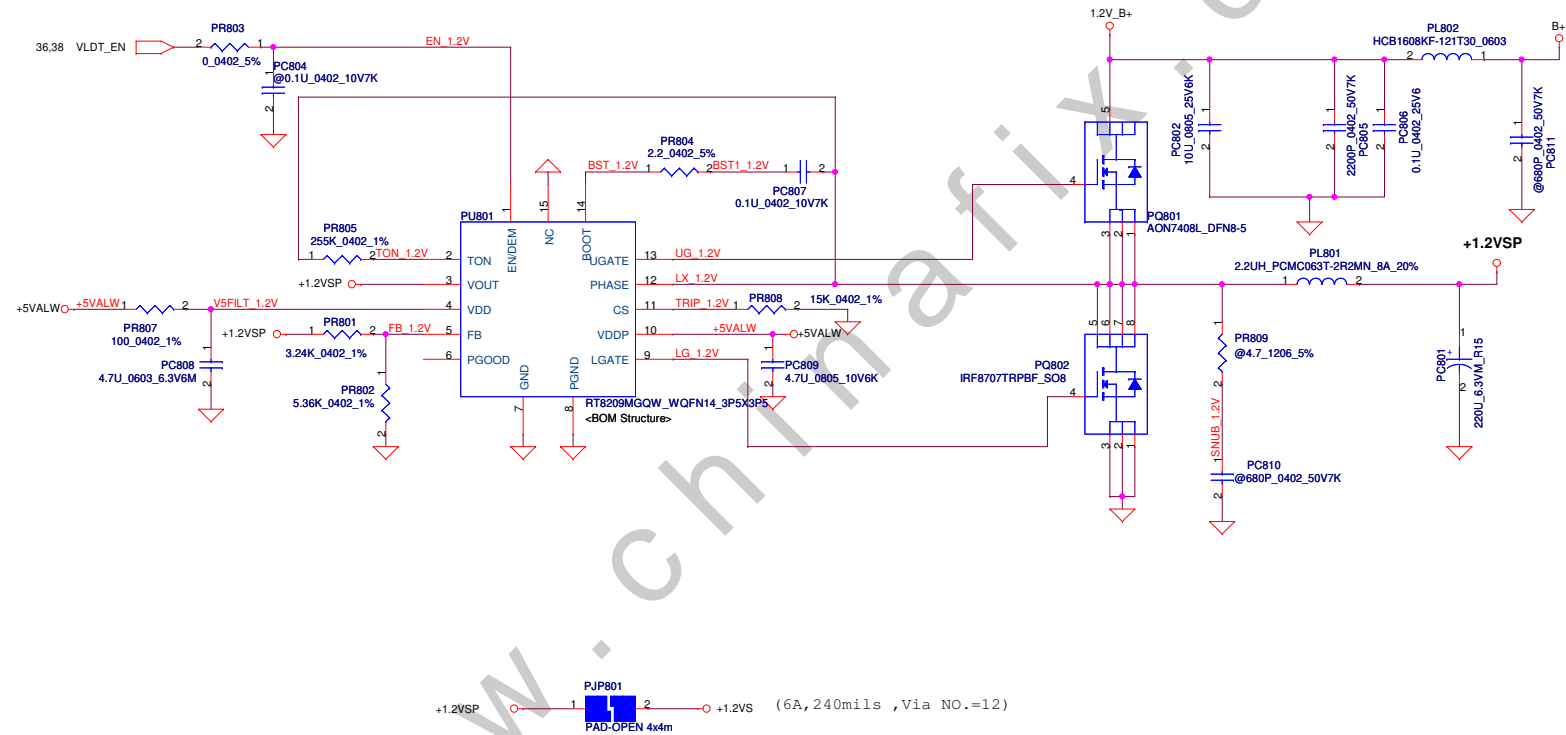


(8A,320mils ,Via NO.= 16)

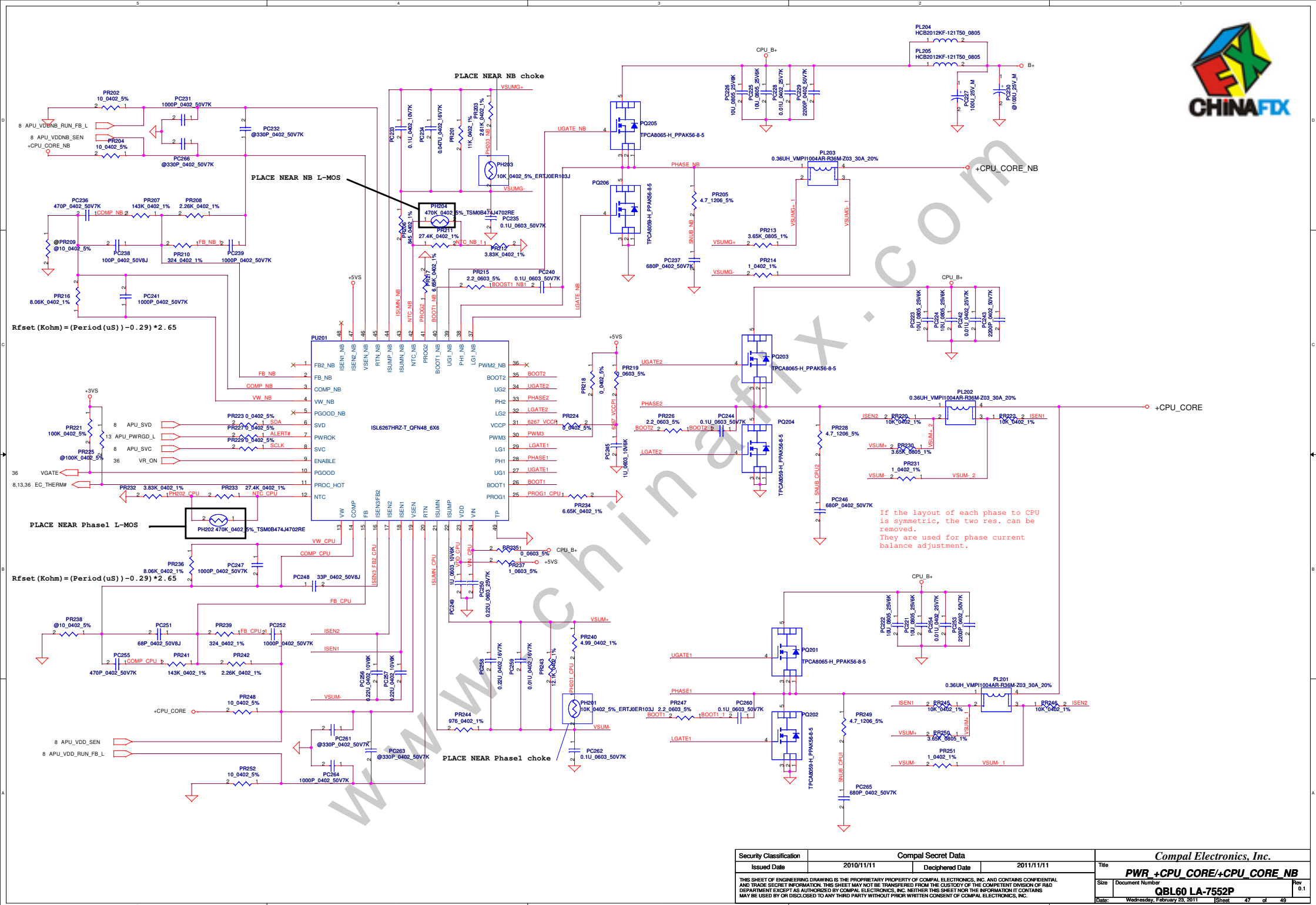
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				Date	Wednesday, February 23, 2011
				Sheet	43 of 49
				Rev	0.1

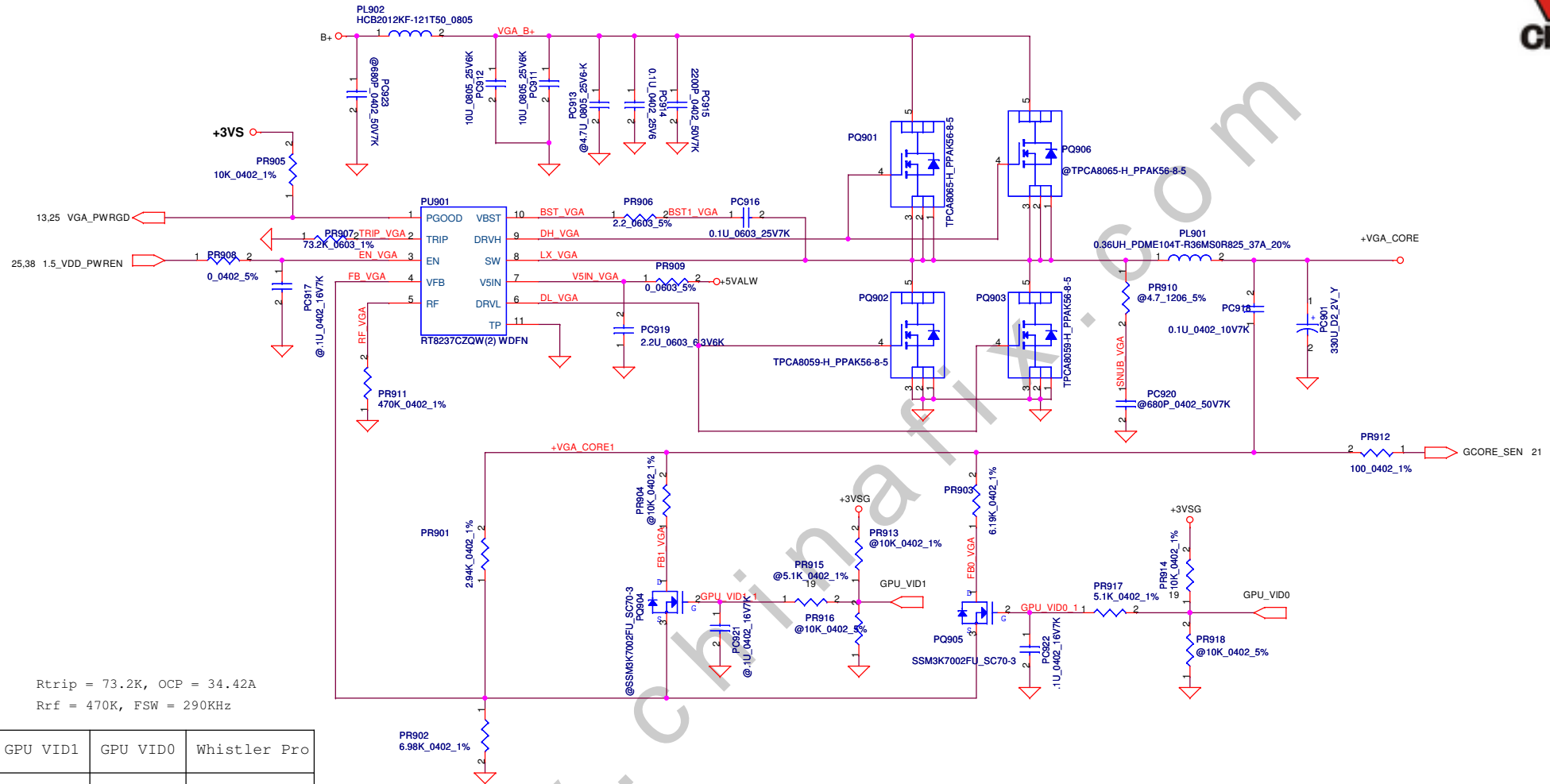


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Issued Date	2009/12/01	Deciphered Date	2010/12/31	Title	PWR+1.1VALWP
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				Date	Wednesday, February 23, 2011
				Sheet	44 of 49
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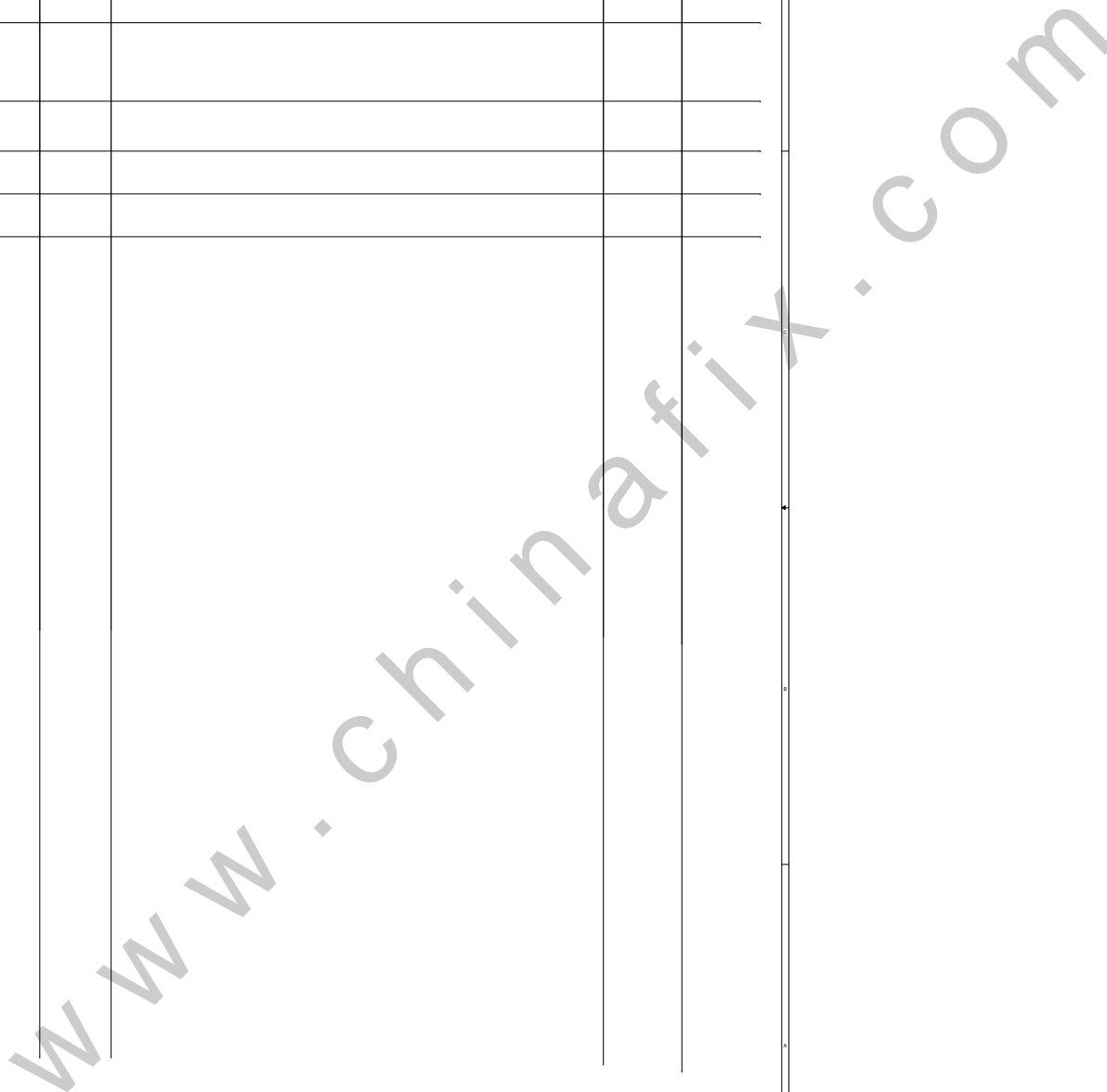


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GPU VID1	GPU VID0	Whistler Pro
X	L	1.0V
X	H	0.9V
H	L	
H	H	



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